

## **Project Specification**

**Project Name: ATLAS Level-1 Calorimeter Trigger-  
VME Mount Module**

**W. Qian**

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### **Distribution for all updates:**

<b>Project Manager:</b>	<b>V. J. O. Perera</b>
<b>Customer:</b>	<b>C. N. P. Gee</b>
<b>Group Leader responsible for Project:</b>	<b>R. N. J. Halsall</b>
<b>Project Managers of related projects:</b>	<b>R. Staley, S. Silverstein, U. Schaefer</b>
<b>Account Manager:</b>	<b>S. P.H. Quinton</b>
<b>Level-1 Trigger Project Manager:</b>	<b>E. Eisenhandler</b>

# Table of Contents

Table of Contents .....	2
Document History .....	2
<b>1 Scope .....</b>	<b>3</b>
<b>2 Related projects and documents .....</b>	<b>3</b>
<b>3 Technical Aspects .....</b>	<b>3</b>
3.1 Requirements, Specifications and Implementations .....	4
3.1.1 Mechanical requirements .....	4
3.1.2 Second ethernet port .....	4
3.1.3 Line impedance .....	4
3.1.4 Signal Termination.....	4
3.1.5 VME-- signal generation .....	7
3.1.6 Reset signal handling .....	8
3.1.7 Permitted Address Modes .....	8
3.1.8 Front Panel Inputs .....	8
3.1.9 Front Panel Indicator LEDs .....	8
3.1.10 Power Requirements .....	9
3.1.11 Ground Points .....	9
3.2 Programming Model.....	9
3.3 Testing .....	9
3.3.1 Test Strategy .....	9
3.3.2 Test Equipment .....	9
3.4 Manufacturing .....	10
3.5 Maintenance and further orders.....	10
<b>4 Project Management .....</b>	<b>10</b>
4.1 Personnel .....	10
4.2 Deliverables.....	10
4.2.1 To the Customer:.....	10
4.2.2 From the Customer: .....	10
4.3 Project plan.....	10
4.4 Progress monitoring .....	10
4.5 Training .....	10
4.6 CAE .....	11
4.7 Intellectual Property Rights (IPR) and Confidentiality .....	11
4.8 Safety .....	11
4.9 Environmental impact .....	11
4.9.1 Disposal.....	11
4.9.2 EMC.....	11
4.9.3 Handling.....	11
<b>Appendix: Concurrent SBC VP315 connector P0 Pin-outs.....</b>	<b>A-6</b>
<b>Appendix: Ethernet RJ-45 connector Pin-outs.....</b>	<b>A-13</b>

## Document History

The history of this document is as follows:

- January 2002: Version draft 1 released.
- September 2005: Version 2.3 released
  - Added buffering logic between 6U SBC VME bus and 9U VME—bus
  - Defined “L” shape PCB for VMM
- November 2005: Version 2.4 released
  - Added Ethernet port for concurrent SBC VP315

# 1 Scope

This document describes the specification of production VME Mount Module (VMM).

The Cluster Processor (CP) and Jet Energy Processor (JEP) of ATLAS Level 1 calorimeter trigger are implemented as 9U crates conforming to IEEE 1101.10 specifications. Both CP crates and JEP crates share a common custom Processor backplane (PB). The basic means of configuration and control of CP/JEP crates is a reduced VME bus (named VME--) accessed from the Processor Backplane.

The VME Mount Module (VMM) accommodates a 6U VME single-board computer (SBC) within a 9U CP/JEP crate and bridges the standard VME bus on the 6U SBC to VME-- on the Processor Backplane.

# 2 Related projects and documents

2.1 ATLAS TDR at <http://atlasinfo.cern.ch/Atlas/GROUPS/DAQTRIG/TDR/tdr.html>

2.2 CPM specification at <http://hepwww.rl.ac.uk/Atlas-L1/Modules/Modules.html>

2.3 JEM specification at <http://hepwww.rl.ac.uk/Atlas-L1/Modules/Modules.html>

2.4 Processor Backplane specification at <http://hepwww.rl.ac.uk/Atlas-L1/Modules/Components.html>

2.5 Reduced VME specification at <http://hepwww.rl.ac.uk/Atlas-L1/TIN/TIN.htm>

# 3 Technical Aspects

The VMM is a 9U VME-- module, with an enclosed slot for a 6U VME standard SBC. The conceptual layout of the VMM is shown in Figure 1.

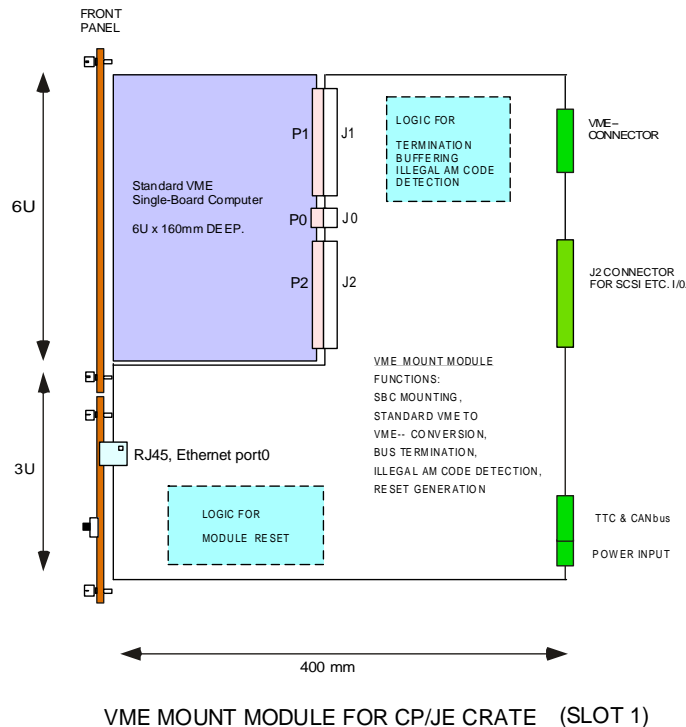


Figure 1: VME Mount Module overview.

### **3.1 Requirements, Specifications and Implementations**

The VMM module physically houses a 6U SBC. Due to the signal conversion between standard VME and VME-- and the reduced functionality and signal availability of VME--, the VMM is implemented as a VME master only. This means that NO two VMMs should be inserted into a single CP/JEP crate at the same time, although two CPU slots are provided within each CP/JEP crate. Meanwhile, no interrupt handling mechanism is provided on the VMM.

The main tasks of the VMM are:

- Mechanically supports a 6U SBC in the 9U processor crate.
- Provides standard terminations for all VME signals on 6U SBC.
- Provides proper termination for CAN bus on 9U processor backplane.
- Provides proper terminations for VME-- signals on 9U processor backplane.
- Provides required buffers between +5V VME signals on 6U SBC J1 and +3.3V VME-- signals on 9U processor backplane.
- Connects all signals from 6U SBC J2 to the J2 connector on 9U processor backplane respectively.
- Connects proper geographic address pins from 9U backplane to 6U SBC.
- Detects and aborts VME cycles other than A24D16.
- Provides additional system reset function.
- Provides required power supplies to 6U SBC and on-board logic.
- Provides an 8-way RJ45 socket on the front panel to accommodate second Ethernet port to the Concurrent 6U SBC VP315 via P0/J0 connector.

#### ***3.1.1 Mechanical requirements***

The mechanics on the VMM that hold a 6U SBC should be precisely implemented according to VME standard so that a 6U SBC can easily be inserted into and mate with the VMM. If possible, a plastic protection cover sheet should be attached to the bottom side of the VMM to avoid short circuit in slot 1 position.

#### ***3.1.2 Second Ethernet port***

The Concurrent 6U SBC VP315 has it “Ethernet Port 0” available on it P0 connector. An 8-way RJ45 socket is provided on the VMM front panel to bring out this “Ethernet Port 0” through P0/J0 connection. This RJ45 socket will not provide Ethernet connectivity for other models of Concurrent SBC, in particular VP-110.

#### ***3.1.3 Line impedance***

The VMM module is an impedance-controlled PCB. The differential impedance of the 4 ethernet signal pairs on the VMM is specified to be  $100\Omega \pm 10\%$ . The impedance of all other signal tracks on the VMM is specified to be  $60\Omega \pm 10\%$ .

#### ***3.1.4 Signal Termination***

In principle, termination networks should be used on all 6U VME and 9U VME-- signals except the daisy-chain lines (BGxIN\*, BGxOUT\*, IACKIN\* and IACKOUT\*) and serial bus lines (SERA and SERB). The basic termination network used on the VMM and its Thevenin equivalent is shown in Figure 2.

DS0\* and DS1\* from 6U SBC are the most critical timing signals. Timing for all address and data transfers are measured with respect to these two signals. In order to

minimize signal reflections, the termination network shown in Figure 3 is used on the VMM for DS0\* and DS1\*, where the resistance values are halved compared to Figure 2.

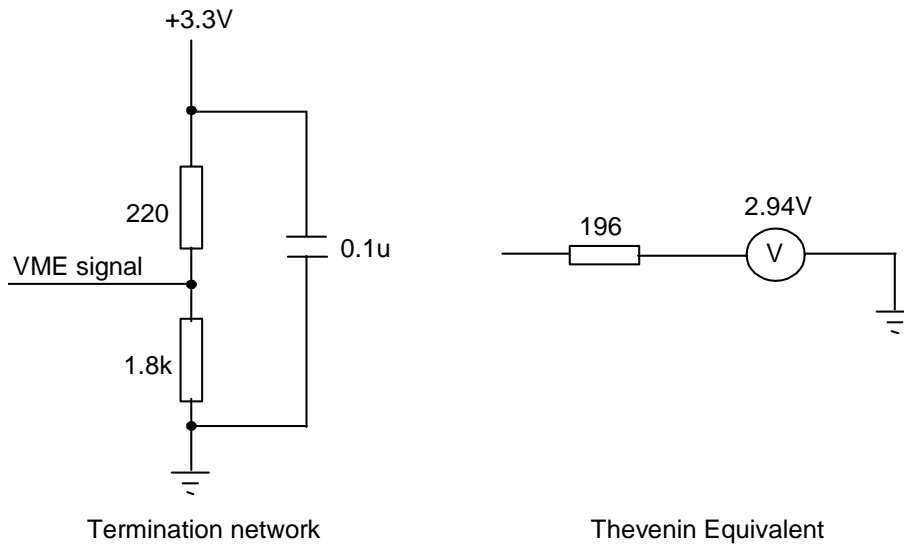


Figure 2: VMM basic signal termination network.

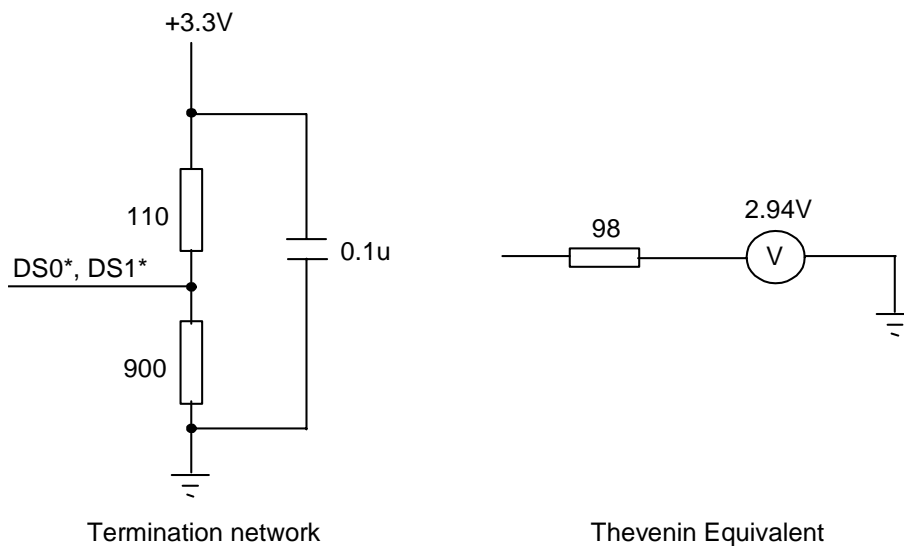


Figure 3: Termination network for DS0\* and DS1\* on VMM

Several termination topologies are used on the VMM for 6U VME and 9U VME-- signals as shown in Figure 4.

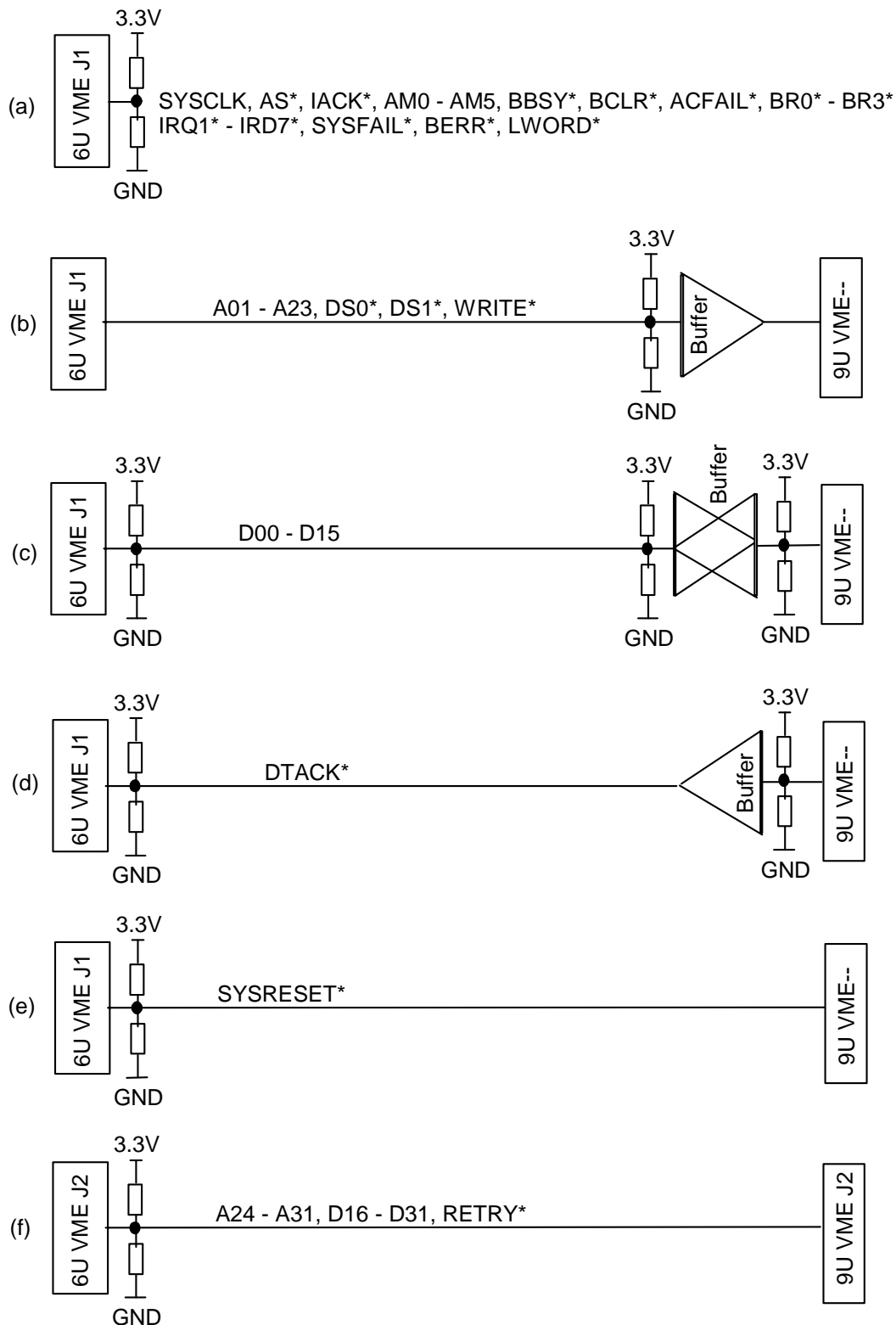


Figure 4: VMM signal termination topologies and buffer scheme.

(a) For 6U VME signals SYSCLK, AS\*, IACK\*, AM0 - AM5, BBSY\*, BCLR\*, ACFAIL\*, BR0\* - BR3\*, IRQ1\* - IRD7\*, SYSFAIL\*, BERR\* and LWORD\*, which are not used on the 9U processor backplane, only one termination network is used for each signal. The termination is placed close to the 6U SBC VME connector J1.

(b) For 6U VME signals A01-A23, DS0\*, DS1\* and WRITE\*, only one termination is used for each signal, which is placed close to the buffer which converts it into 9U VME--. After the buffer, no termination is needed on the VMM side for 9U VME-- signals A01-A23, DS\* and WRITE\*.

(c) For 6U VME signals D00-D15, a termination is used at each end of each signal track. For 9U VME-- signals D00-D15, one termination is used on the VMM side for each signal.

(d) For 6U VME signal DTACK\*, one termination is placed close to the 6U SBC VME connector J1. For 9U VME-- signal DTACK\*, one termination is used on the VMM side.

(e) 6U VME SYSRESET\* connects directly to 9U VME-- SYSRESET\*. One termination is placed close to 6U SBC VME connector J1.

(f) Signals on 6U SBC VME J2 connect directly to 9U VME J2. One termination is used for each signal, which is placed close to 6U SBC VME connector J2.

### 3.1.5 VME-- signal generation

The VME-- bus on the 9U processor backplane consists of the 50 signals shown in Table 1:

Signal mnemonic	Name	Pins
A01-A23	Address bus	23
DS*	Data strobe	1
D00-D15	Data bus	16
DTACK*	Data transfer acknowledge	1
WRITE*	Read/Write	1
SYSRESET*	System reset	1
GA0-GA6	Geographical Address	7

Table 1: VME-- signal list.

VME-- signals are generated as follows:

VME-- A01-A23 are simply buffered from 6U VME A01-A23.

VME-- DS\* is generated by an “OR” gate ORing DS0\* and DS1\* from 6U VME.

VME-- D00-D15 are bi-directionally buffered from 6U VME D00-D15. The buffer direction is controlled by WRITE\* from 6U VME.

VME-- DTACK\* is buffered (using an open-collector gate) to 6U VME DTACK\*.

VME-- WRITE\* is simply buffered from 6U VME WRITE\*.

VME-- SYSRESET\* connects directly to 6U VME SYSRESET\*.

VME-- GA0-GA6 are hardwired on the 9U processor backplane. VME-- GA0 is directly connected to 6U VME GA0\*. 6U VME GA1\*-GA4\* and GAP\* are left open on VMM. When a 6U SBC plus VMM is inserted into slot 1 of a CP/JEP crate, GA0\* will be pulled to ground by the backplane while GA1\*-GA4\* are open. The 6U SBC

interprets this code to indicate slot 1. When a 6U SBC plus VMM is inserted into slot 2 of a CP/JEP crate, GA0\* is not pulled to ground by the backplane, so all signals GA0\*-GA4\* are open. The SBC will interpret this code as a legacy backplane without geographical addressing.

### 3.1.6 Reset signal handling

Normally, the 6U SBC resets the whole CP/JEP crate during power-up or reboot as the 6U SBC SYSRESET\* connects directly to the 9U VME-- SYSRESET\*. Many 6U SBCs, including the Concurrent series now used in ATLAS, provide an option to disable the generation of SYSRESET\*. In order to maintain flexibility, an additional reset pushbutton is provided on the VMM front panel, which will reset the whole CP/JEP crate including the SBC and all the processor modules when engaged. An option is also provided on the VMM to disable this front panel reset pushbutton.

### 3.1.7 Permitted Address Modes

The SBC is capable of generating VME cycles with a variety of address and data bus widths (A16, A24, A32, D8, D16, and D32). The VME-- backplane supports only A24D16 cycles. To prevent inadvertent use of other address modes, the VMM includes logic to check the VME address modifier (AM) code. The only permitted AM codes are 39 (A24 non-privileged data access) and 3D (A24 supervisory data access). The permitted D16 data width corresponds to DS0\*=DS1\*=0, LWORD\*=1. If the VMM detects any other VME cycle type being attempted, it terminates the cycle by asserting BERR\* to the 6U SBC. In this case, the DS\* signal is not propagated to the VME-- backplane, and no VME-- cycle occurs.

### 3.1.8 Front Panel I/Os

An 8-way RJ45 Ethernet socket and a manual reset pushbutton.

### 3.1.9 Front Panel Indicator LEDs

The status of the VMM is indicated on the front panel by LEDs. Transient signals SYSRESET\* and BERR\* are stretched to a significant fraction of a second to allow it to be visible. Indication of normal module state is green, that of System Reset is yellow and error condition Bus Error is red.

Description	Signal name	Colour
Power supply +5V	+5V	GREEN
Power supply +3.3V	+3.3V	GREEN
Power supply +12V	+12V	GREEN
Power supply -12V	-12V	GREEN
System Reset (Stretched)	SYSRESET*	YELLOW
Bus Error (Stretched)	BERR*	RED
Crate address MSB	GA6	GREEN
Crate address	GA5	GREEN
Crate address LSB	GA4	GREEN
Slot number	GA0	GREEN

Table 2: Front Panel indicator LEDs.

### ***3.1.10 Power Requirements***

The 6U SBC requires +5V. Onboard terminations and buffers require +3.3V. In addition, +12V and -12V may also be needed by PMC cards on the 6U SBC.

+5V supply is directly available from 9U backplane. The +5V power supply to the 6U SBC should stay within the range of 4.875V to 5.25V. Low drop power distribution, preferably solid PCB planes, should be used. No fuse should be used in this power distribution path.

A linear regulator is used to generate +3.3V. Two DC-DC converters are used to generate +12V and -12V. At present no DC-DC converters will be assembled on the VMM since +/-12 V are not currently used.

The total current required from +5V supply is estimated to be ~ 8A.

### ***3.1.11 Testpoints and Ground Points***

Easily accessible testpoints are provided for the following signals:

- 9U VME-- signals: DS\*, DTACK\*, WRITE\*, SYSRESET\*
- 6U SBC VME signals: DS0\*, DS1\*, WRITE\*, DTACK\*, AS\*, BERR\*

Several ground points are provided for scope probe grounding in exposed areas of the module.

## **3.2 Programming Model**

The module has no computer-accessible registers.

## **3.3 Testing**

### ***3.3.1 Test Strategy***

The following tests should be carried out.

1. Stand-alone continuity test of the board
2. Unpowered continuity test with processor backplane.
3. DS\* signal quality check on the 9U VME-- backplane.
4. Single VME cycles from SBC to a target module containing known data.
5. VME soak testing with all slots of a CP/JEP crate populated.

### ***3.3.2 Test Equipment***

1. 9U CP/JEP crate
2. 6U SBC
3. Oscilloscope
4. Logic analyser
5. 6U VME Extenders

### 3.4 Manufacturing

An outside manufacturer will carry out manufacture of the PCBs and the component assembly.

### 3.5 Maintenance and further orders

This module is the production version of VMM and will be used in the final CP/JEP systems of ATLAS L1Calo. In the first instance 2 VMM modules will be produced. 11 further VMM modules will be produced contingent on the successful test of the first 2 VMMs. A total of 13 VMM modules will be available for the final system.

## 4 Project Management

### 4.1 Personnel

		RAL Ext.	RAL Location
Customer:	C. N. P. Gee	6244	R1, 1.39
Project Manager:	V. Perera	5692	R68, 2.31
Project Engineer	W. Qian	6128	R1, 1.36

### 4.2 Deliverables

#### 4.2.1 To the Customer:

1. 2 VMMs.
2. Specification document and User Manual.
3. Schematics.

#### 4.2.2 From the Customer:

Test Software, Powered 9U CP/JEP crate, 6U SBC.

### 4.3 Project plan

- |                                    |                |
|------------------------------------|----------------|
| 1. Preliminary Design Review (PDR) | March, 2001    |
| 2. Final Design Review (FDR)       | November, 2005 |
| 3. Preproduction (2 VMMs)          | January, 2006  |
| 4. Testing of preproduction VMMs   | January, 2005  |
| 5. Production (11 VMMs)            | February, 2006 |
| 6. Testing of production VMMs      | March, 2006    |

### 4.4 Progress monitoring

The progress of the project will be reported in the fortnightly hardware phone conference of the ATLAS L1Calo Trigger project.

### 4.5 Training

Training will be carried out as required on the job.

## **4.6 CAE**

Cadence is used for schematic capture.

## **4.7 Intellectual Property Rights (IPR) and Confidentiality**

All background and foreground Intellectual Property Rights in this project will remain with CCLRC. The customer will have unrestricted rights to items listed under deliverables (4.2). If the customer requires other data, then an appropriate protective agreement should be in place before releasing such data.

## **4.8 Safety**

General laboratory safety codes apply.

## **4.9 Environmental impact**

### ***4.9.1 Disposal***

RAL will dispose of the modules at end of their life.

### ***4.9.2 EMC***

Appropriate EMC design rules should be used in the VMM PCB design.

### ***4.9.3 Handling***

Anti-static precautions must be taken when handling the module to prevent damage to components.

## SPECIFICATIONS

### A.5.3 PMC I/O Connector (P0) Pin-outs

This is a 95-way (5-row x 19-position) IEC 61076-4-101 2mm pitch connector. It carries all 64 I/O signals from the PMC Site 2 and Ethernet channels 1 and 2 (if configured). The pin assignments conform to the Ethernet mapping defined in the ANSI/VITA 31.1 standard and are shown below.

Position	Row F	Row E	Row D	Row C	Row B	Row A
1	GND	-	-	-	-	-
2	GND	ETH0_DC-	ETH0_DC+	GND	ETH0_DA-	ETH0_DA+
3	GND	ETH0_DD-	ETH0_DD+	GND	ETH0_DB-	ETH0_DB+
4	GND	PI02_1	PI02_2	PI02_3	PI02_4	PI02_5
5	GND	PI02_6	PI02_7	PI02_8	PI02_9	PI02_10
6	GND	PI02_11	PI02_12	PI02_13	PI02_14	PI02_15
7	GND	PI02_16	PI02_17	PI02_18	PI02_19	PI02_20
8	GND	PI02_21	PI02_22	PI02_23	PI02_24	PI02_25
9	GND	KBD_DA	KBD_CLK	GND	MS_CLK	MS_DA
10	GND	RED	AGND	GREEN	AGND	BLUE
11	GND	DDCDA	DDCCK	VSYNC	AGND	HSYNC
12	GND	PI02_26	PI02_27	PI02_28	PI02_29	PI02_30
13	GND	PI02_31	PI02_32	PI02_33	PI02_34	PI02_35
14	GND	PI02_36	PI02_37	PI02_38	PI02_39	PI02_40
15	GND	PI02_41	PI02_42	PI02_43	PI02_44	PI02_45
16	GND	PI02_46	PI02_47	PI02_48	PI02_49	PI02_50
17	GND	PI02_51	PI02_52	PI02_53	PI02_54	PI02_55
18	GND	PI02_56	PI02_57	PI02_58	PI02_59	PI02_60
19		PI02_61	PI02_62	PI02_63	PI02_64	GPIO1

**Table A-4 P0 Pin-out for PMC I/O, Keyboard, Mouse, VGA, GPIO**

Position	Row F	Row E	Row D	Row C	Row B	Row A
1	GND	-	-	-	-	-
2	GND	ETH0_DC-	ETH0_DC+	GND	ETH0_DA-	ETH0_DA+
3	GND	ETH0_DD-	ETH0_DD+	GND	ETH0_DB-	ETH0_DB+
4	GND	ETH1_DC-	ETH1_DC+	GND	ETH1_DA-	ETH1_DA+
5	GND	ETH1_DD-	ETH1_DD+	GND	ETH1_DB-	ETH1_DB+
6	GND	GND OR -	GND OR -	GND OR -	GND OR -	GND OR -
7	GND	SATA0_RX-	SATA0_RX	GND	SATA0_TX	SATA0_TX
8	GND	GND	GND	GND	GND	GND
9	GND	KBD_DA	KBD_CLK	GND	MS_CLK	MS_DA
10	GND	RED	AGND	GREEN	AGND	BLUE
11	GND	DDCDA	DDCCK	VSYNC	AGND	HSYNC
12	GND	USB_DA2+	USB_DA2-	GND	GPIO2	GND
13	GND	USB_PWR	GND	PI02_33	PI02_34	PI02_35
14	GND	PI02_36	PI02_37	PI02_38	PI02_39	PI02_40
15	GND	PI02_41	PI02_42	PI02_43	PI02_44	PI02_45
16	GND	PI02_46	PI02_47	PI02_48	PI02_49	PI02_50
17	GND	PI02_51	PI02_52	PI02_53	PI02_54	PI02_55
18	GND	PI02_56	PI02_57	PI02_58	PI02_59	PI02_60
19	GND	PI02_61	PI02_62	PI02_63	PI02_64	GPIO1

**Table A-5 P0 Pin-out for VITA 31.1, Keyboard, Mouse, I/O 33..64**

**NOTE:** This connector is a build time option and is not available on all variants.

