

The Temperature Dependence of the Electrical Performance of ABCD2T readout chips in Prototype ATLAS SCT Barrel Modules

Aidan Robson, Peter W. Phillips *
Rutherford Appleton Laboratory

September 15, 2000

Abstract

Several aspects of ATLAS SCT module temperature dependence have been investigated using two SCT Barrel prototype modules within an environmental chamber with a nitrogen flow. The modules, equipped with ABCD2T readout chips, showed the noise to change by $0.04 \pm 0.01 \text{mV } ^\circ\text{C}^{-1}$ or $5 \pm 1 \text{ENC } ^\circ\text{C}^{-1}$.

1 Introduction

As the readout chips on SCT barrel modules are to be run at temperatures around 0°C , yet are required to be operational across a wide temperature range from -25°C to $+80^\circ\text{C}$, it is important to understand the temperature dependencies of their operating characteristics.

An environmental chamber with a flow of nitrogen has been used to study two SCT barrel modules built with unirradiated detectors and using ABCD2T readout chips (Ref. [a]). Some thermal properties of the hybrid-baseboard-box system are investigated, followed by module electrical characteristics: behaviour of the chip strobe delay register, gain and noise.

*The collaboration with SCT UK-Barrel colleagues at Cambridge, QMW, RAL and Birmingham, with the SCT Oslo group and with CERN EST Division is gratefully acknowledged.

2 System thermal properties

Temperature differences across the system Figure 1 shows one such module, module "A" (Ref. [b]), and its temperature sensors. The module has 12 ABCD2T readout chips mounted on a hybrid with an integrated TPG substrate (Ref. [c,d]) and constructed with a TPG/BeO internal baseboard (Ref. [c,d]). It is equipped with a SemiTec thermistor (Ref. [e], Fig. 1 label 1). A Pt1000 sensor (label 2) was mounted on the top BeO facing of the baseboard close to where the thermal connection to the box is made, and another Pt1000 sensor (label 3) mounted on the frame of the aluminium box.

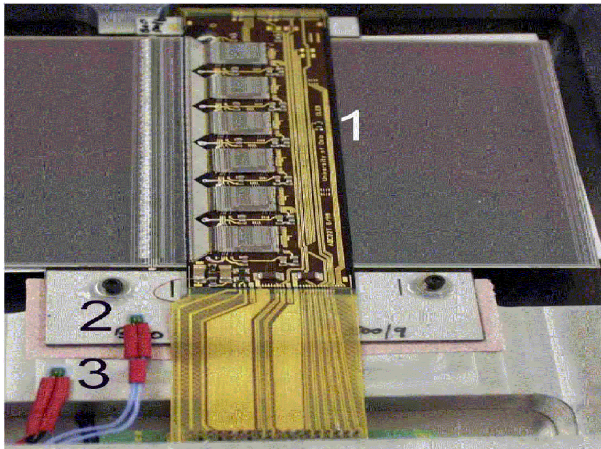


Figure 1: Module "A" showing the position of the upper hybrid, its thermistor (1) and two Pt1000 sensors (2,3)

For illustration, figure 2 shows the difference between hybrid, baseboard and box temperatures and the chamber temperature under steady state conditions at various chamber temperatures. Each point shows the average and standard deviation of three consecutive measurements, separated by one minute.

It is seen that the hybrid, baseboard and box retain an almost constant difference between them, and that at low chamber temperatures the difference between each of these and the chamber increases slightly with decreasing chamber temperature. This increase is caused by the nitrogen flow through the box, which at very low chamber temperatures does not cool sufficiently to reach the

chamber temperature before passing over the module.

While the module and box reach a steady temperature, the chamber rises several degrees between bursts of chilling, accounting for the discrepancies between points around the same chamber temperature.

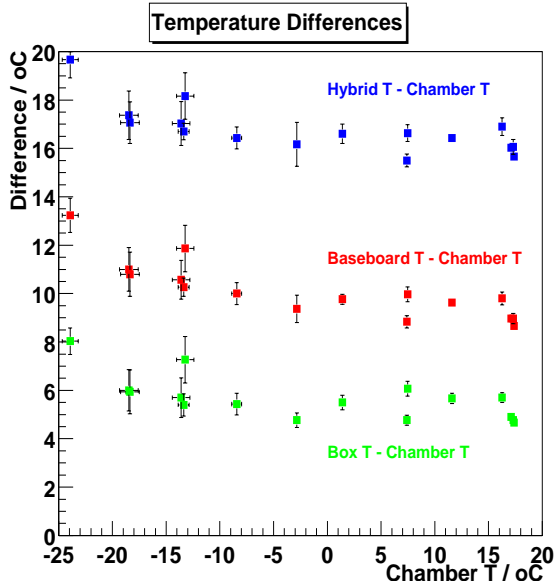


Figure 2: Steady-state differences from chamber temperature

Baseboard-box thermal contact As an attempt to improve thermal contact between the module baseboard and the box, a piece of KTP 127-NA (Ref. [f]) thermally doped silicon rubber, and then of the double-thickness KTP 254-NA, was placed between the baseboard and box. The temperatures of the hybrid, baseboard and box were then measured from power-up, and are shown in Figure 3.

KTP 127-NA resulted in a slight worsening in thermal contact; this is not shown on the plot. However the slightly reduced temperatures of the hybrid and baseboard, and increased temperature of the box with the sheeting compared to without, show that the thicker sheeting does increase the thermal contact. Partial removal of the lid allowed extra convective cooling of the module, shown in the third set of lines.

A subsequent study (Ref. [g]) measured the thermal resistance of a facing-box joint to be $2.1^{\circ}\text{C W}^{-1}$, a joint with the thinner KTP 127-NA material to be $3.0^{\circ}\text{C W}^{-1}$, and a joint with grease to be $0.4^{\circ}\text{C W}^{-1}$. The probable explanation for the worsening with the thin rubber sheeting lies in the extent to which the screws on a facing can be tightened compared to the pressure required for the sheeting to become effective. Thermally conductive grease is clearly a more

Module "A" Thermally Conductive Sheet Tests

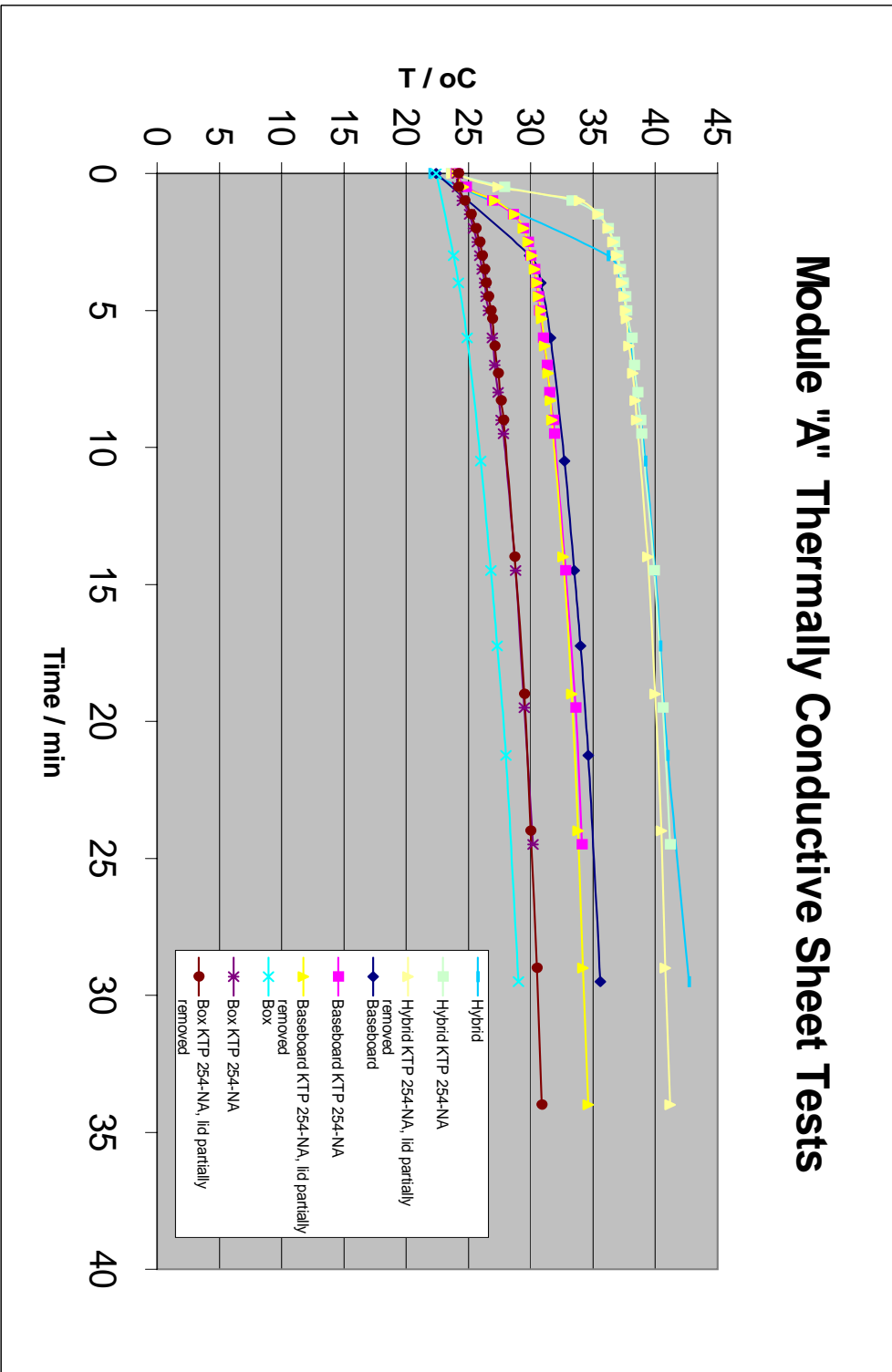


Figure 3: Temperature History of an uncooled module from power-up

appropriate solution, however as a greased module could be difficult to remove the thicker thermally doped silicon rubber sheeting was left in place.

3 Module "A" Noise

A series of scans was taken at several temperatures, in order to examine the variation with temperature of the noise measured. During these electrical studies the module was powered by floating, linear bench supplies. Module readout and data acquisition were performed within the ATLAS SCT TestDAQ environment (Ref. [h]).

At each temperature threshold scans were taken with 2 fC and 3 fC calibration pulses. The gain was approximated as $d \text{ mV fC}^{-1}$ where d (mV) is the difference in the means of the resulting fitted curves; then the noise (fC) was taken to be the average noise (mV) for these two scans divided by the gain, where the noise (mV) for one run was taken to be the width of the s-curve. Noise (fC) is conveniently converted to units of electronic charge (ENC).

It was found that chips tended to fall into two categories, as shown by a few example chips in Figure 4: those like chips 6 and 10, which show a reasonably linear variation of noise with temperature and give a slope of around 4 or 5 ENC $^{\circ}\text{C}^{-1}$, and those like chips 7 and 11, for which the noise increases rapidly at higher temperatures. The error on the noise measurements is around ± 30 ENC.

The two symbols on the figure indicate data collected on two consecutive days, it is also seen that there is a discrepancy between the two sets. However within each day measurements were taken both on cooling and on warming the module, and the reasonable agreement of data within a day would seem to discount a temperature hysteresis effect.

A previous investigation had suggested that the strobe delay setting¹ could change with temperature. The results of a study of the gain of chip 6 as a function of the setting of the delay register, at three different temperatures, are shown in Figure 5. The gain shows a dependence on the delay setting that is further dependent on temperature.

This indicated that in order to obtain a correct set of noise measurements at different temperatures, other parameters would also have to be adjusted. This was further investigated with a second module.

¹This register is used to adjust the timing of the charge injection pulse. Each step is of order 1.2 nS.

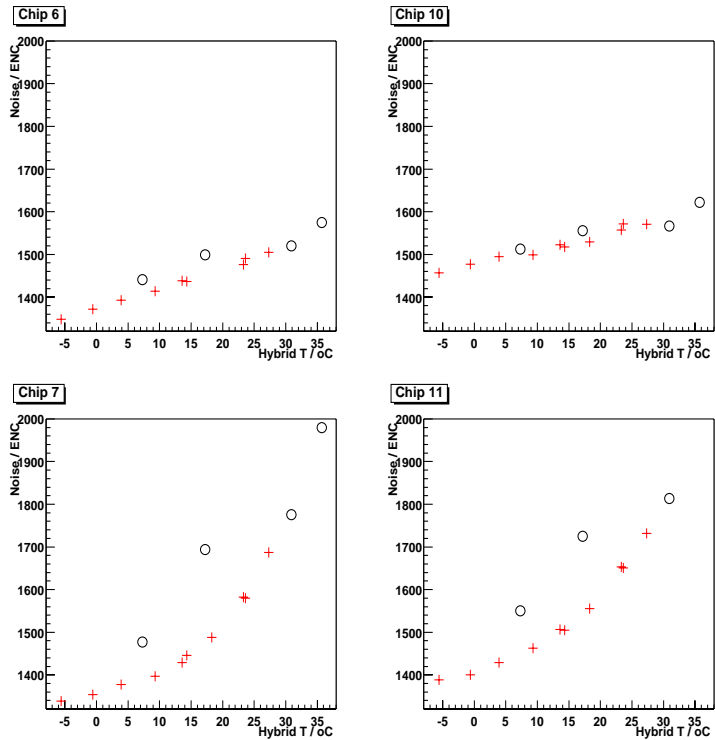


Figure 4: Module "A" noise (ENC) for chips 6,10,7 and 11

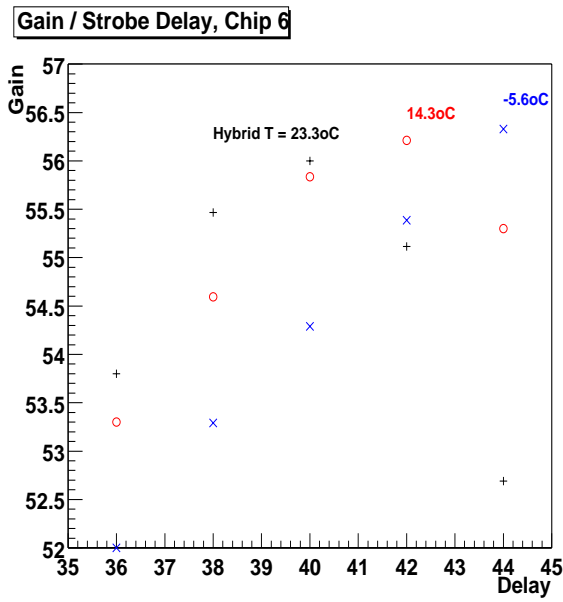


Figure 5: Factors affecting gain (Module "A" chip 6): strobe delay and temperature

4 Module "B" Strobe Delay, Gain and Noise

A further series of temperature-dependent measurements was taken on module "B" (Ref. [i]) which has the same thermo-mechanical features as module "A". It is equipped with two SemiTec thermistors - one on each side of the module - of which only the top device was read out.

The first aim was to factor out the effect of temperature on the strobe delay setting, seen in the data from module "A". Gain and noise measurements were made at a variety of temperatures, at each temperature over a series of strobe delay settings.

Having defined the 'optimum' setting of the delay register at a given temperature to be that at which the gain was maximised, the optimised delay settings for each chip are shown in Figure 6. The other plots show the gain and noise measurements made at this optimum delay setting for each chip at each temperature.

The three marker styles indicate data taken on three consecutive days - the inconsistency seen during earlier studies with module "A" was not repeated. In addition, by taking the most appropriate delay setting the very strong dependence of noise on temperature shown by chips 7 and 11 in Figure 4 was eliminated.

It can be seen that the measured gain, output noise and input noise all vary with temperature. A summary of the fit results for the gain and noise plots of Figures 7, 8 and 9 is given in Table 1. A simple mean of the slopes is shown for the top and bottom sides of the hybrid, and also for the first ten chips only, thereby excluding the less highly performant chips 10 and 11.

Considering only the first ten chips gives a variation of $5 \pm 1 \text{ ENC } ^\circ\text{C}^{-1}$, or $0.04 \pm 0.01 \text{ mV } ^\circ\text{C}^{-1}$, and $-0.18 \pm .02 \text{ delay register steps } ^\circ\text{C}^{-1}$.

	Optimum Delay	Gain	Output Noise	Input Noise
Top hybrid	-0.18 ± 0.02	-0.05 ± 0.03	0.04 ± 0.01	4.9 ± 0.8
Bottom hybrid	-0.16 ± 0.02	-0.23 ± 0.05	0.04 ± 0.02	6.1 ± 1.2
Chips 0-9	-0.18 ± 0.02	-0.06 ± 0.03	0.04 ± 0.01	5.1 ± 0.9
	steps $^\circ\text{C}^{-1}$	$\text{mV fC}^{-1} ^\circ\text{C}^{-1}$	$\text{mV } ^\circ\text{C}^{-1}$	$\text{ENC } ^\circ\text{C}^{-1}$

Table 1: Results summary

5 Conclusions

It is found that for the ABCD2T chips as used in these prototype modules, the setting of the strobe delay register required to maximise the gain has a variation of $-0.18 \pm .02$ delay register steps $^{\circ}\text{C}^{-1}$. Maximising the gain in this way, a change in noise of $0.04 \pm 0.01\text{mV } ^{\circ}\text{C}^{-1}$ or $5 \pm 1\text{ENC } ^{\circ}\text{C}^{-1}$ is observed.

Studies of the properties of the interface between the lower BeO facing and a cooling surface indicated the need for thermal grease.

6 References

[a] ABCD2T/ABCD2NT ASIC, Project Specification V2.1:
http://atlasinfo.cern.ch/Atlas/GROUPS/INNER_DETECTOR/SCT/docs/abcd2.1

[b] Module RLT2

[c] Novel Thermal Management Structures and their Applications in New Hybrid Technologies and Feed-Through Structures, A.A.Carter, R. de Oliveira, A. Gandi, CERN Report 99-08 [13/09/99] (ISBN 92-9083-152-9)

[d] Thermal Management Systems, Patent Applications: A.A.Carter, R. de Oliveira, A. Gandi, UK Applications: (1) 9814835.6 [08/07/1998], (2) 9825376.8 [19/11/1998], (3) 9900924.3 [15/01/1999]; International Application: PCT/GB99/02180 [08/07/1999]

[e] SemiTec thermistor, Part no. 103KT1608-1P:
<http://www.semitec.co.jp>

[f] KTP 127-NA and KTP 254-NA rubber sheeting from Warth International:
<http://www.warth.co.uk>

[g] R.J.Apsimon, private communication

[h] SCT TestDAQ, J.C.Hill, G.F.Moorhead, P.W.Phillips:
<http://s.home.cern.ch/s/sct/public/sctdaq/sctdaq.html>

[i] Module RLT8

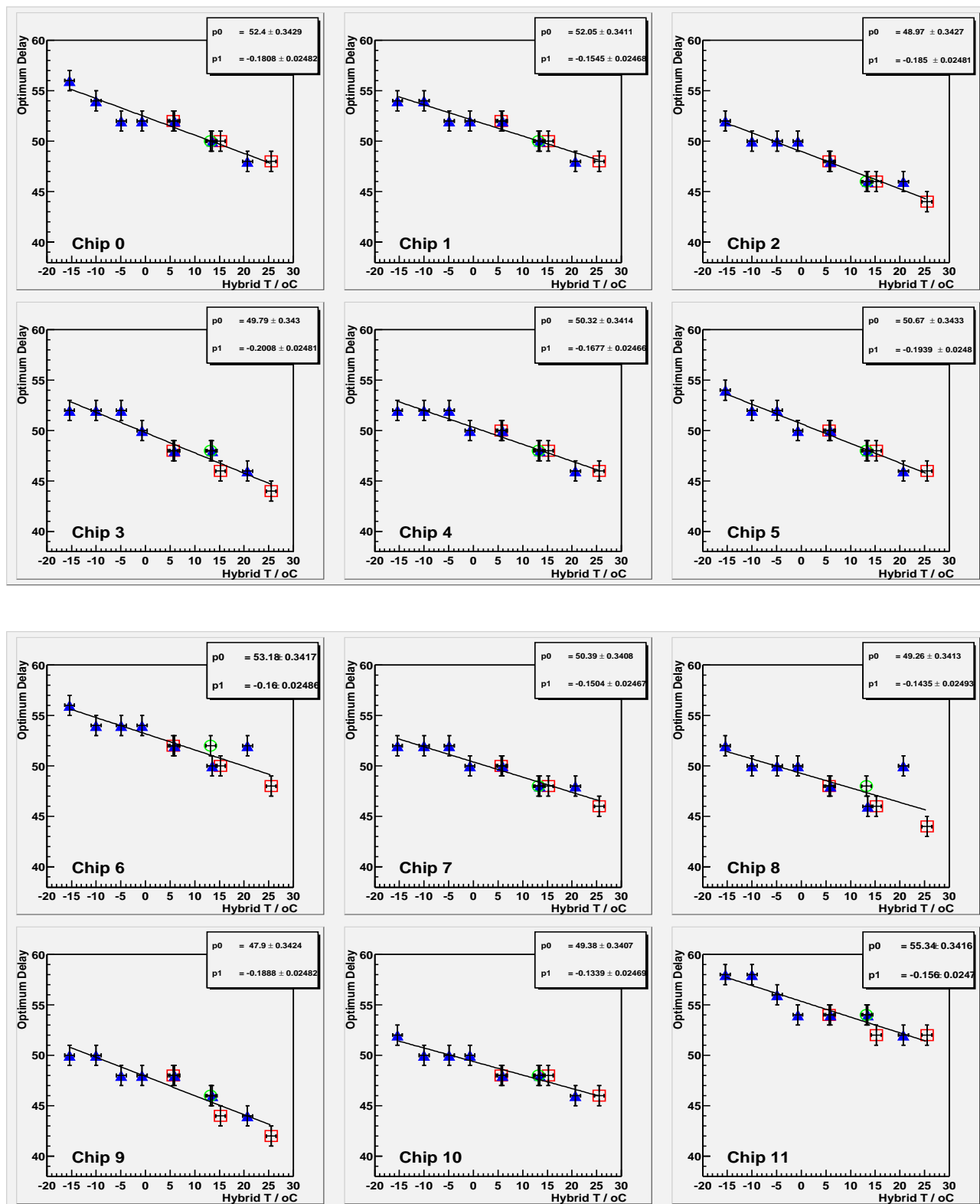


Figure 6: ‘Optimised’ delay settings (see text)

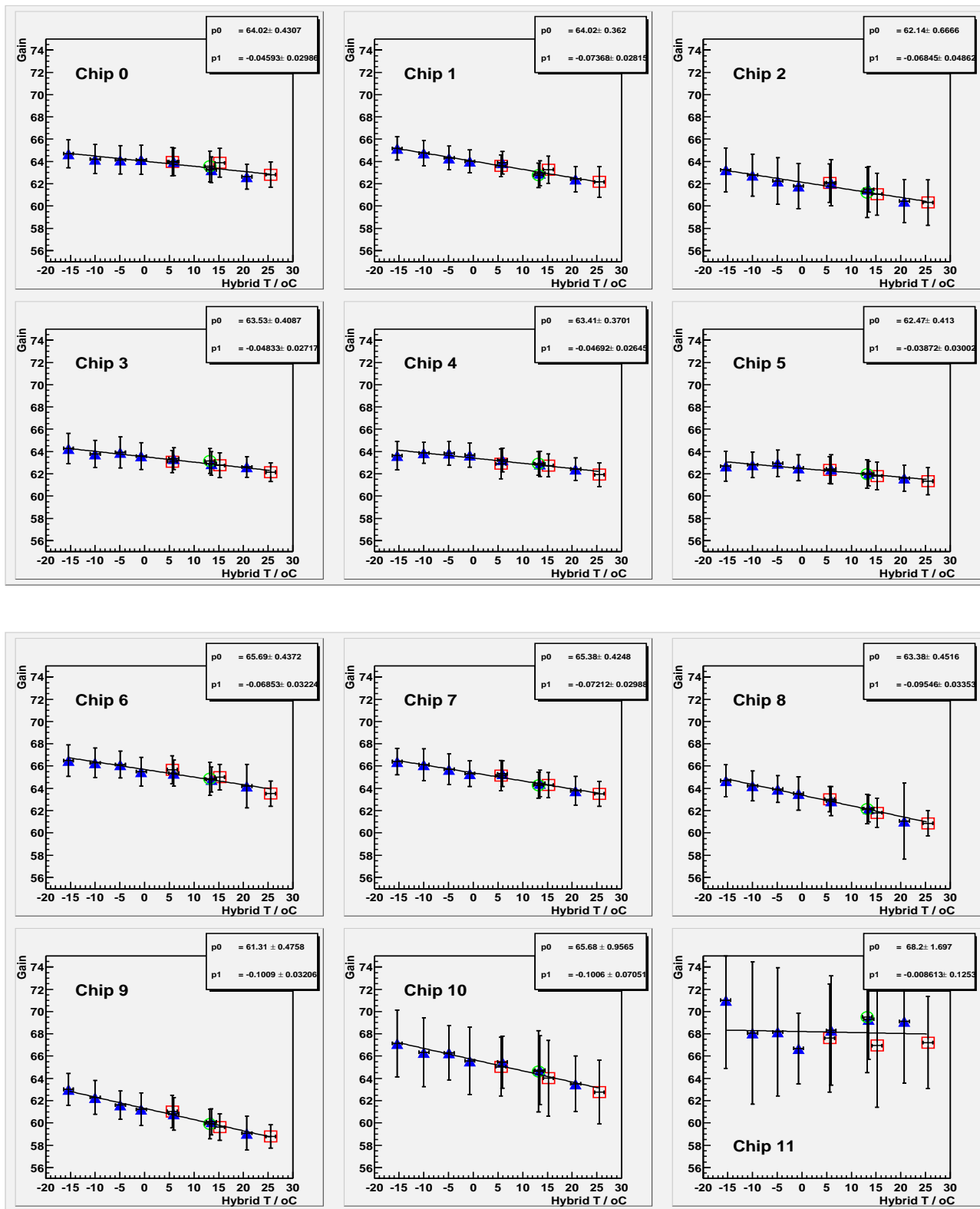


Figure 7: Maximised Gain

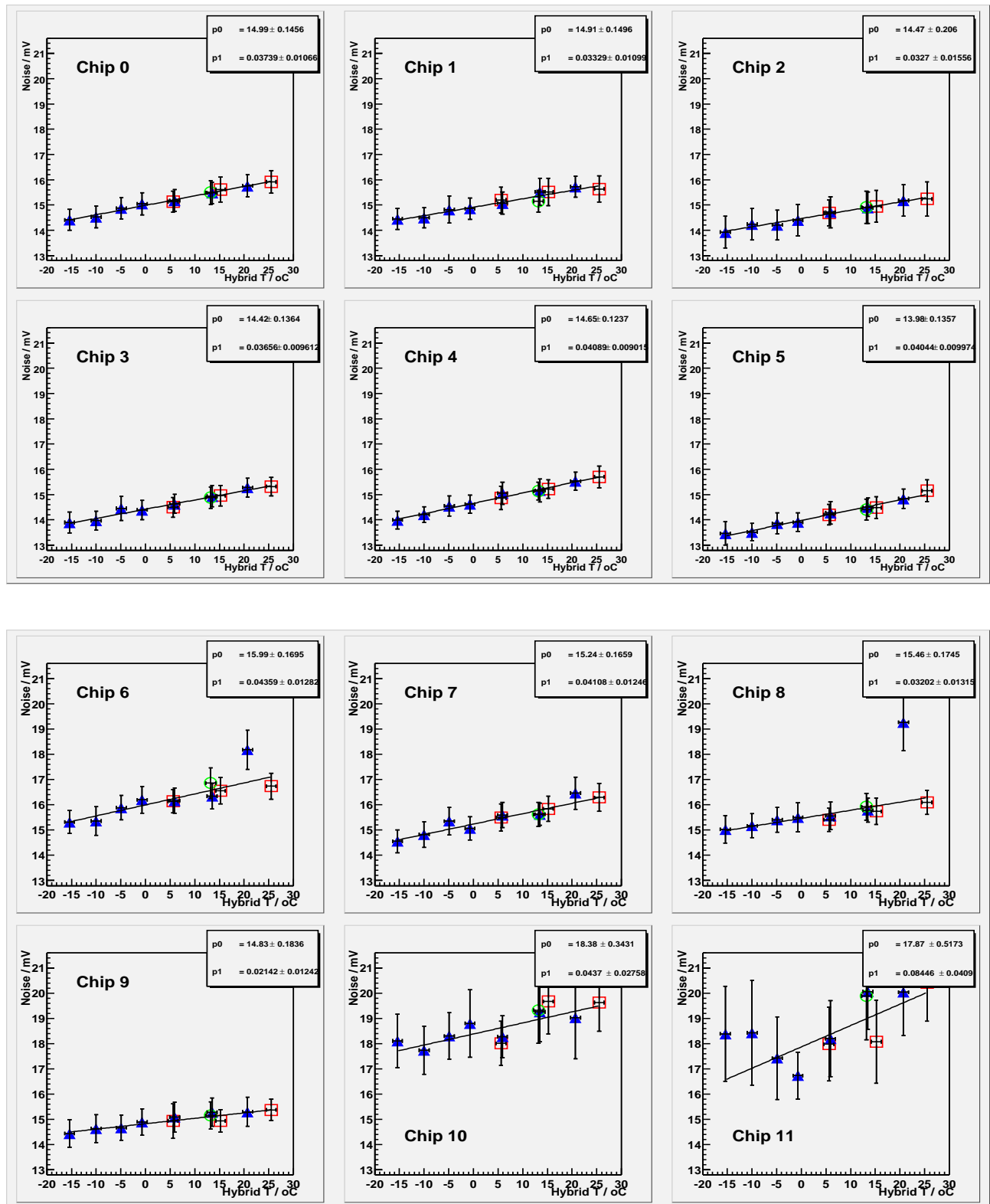


Figure 8: Output Noise (mV)

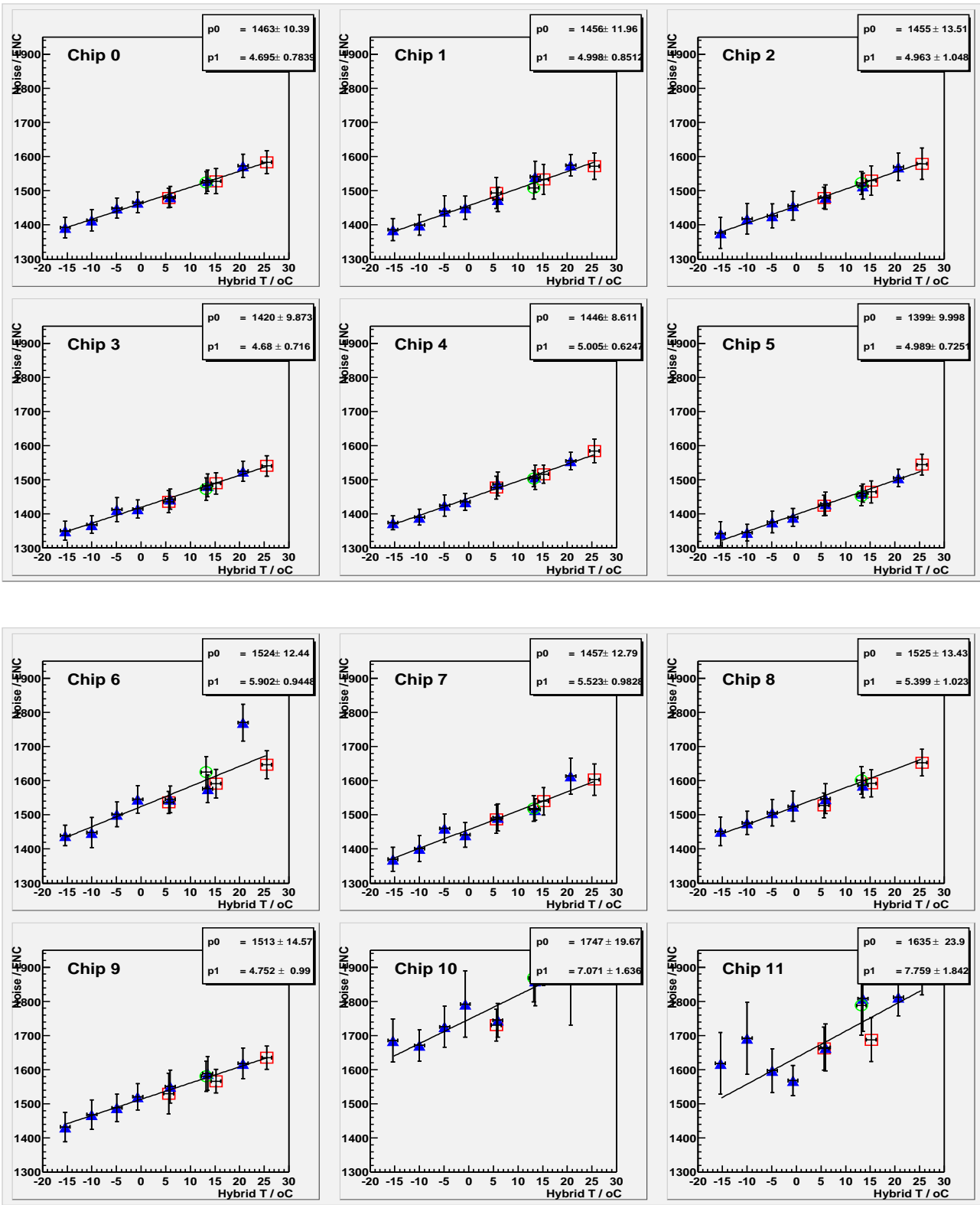


Figure 9: Input Noise (ENC)