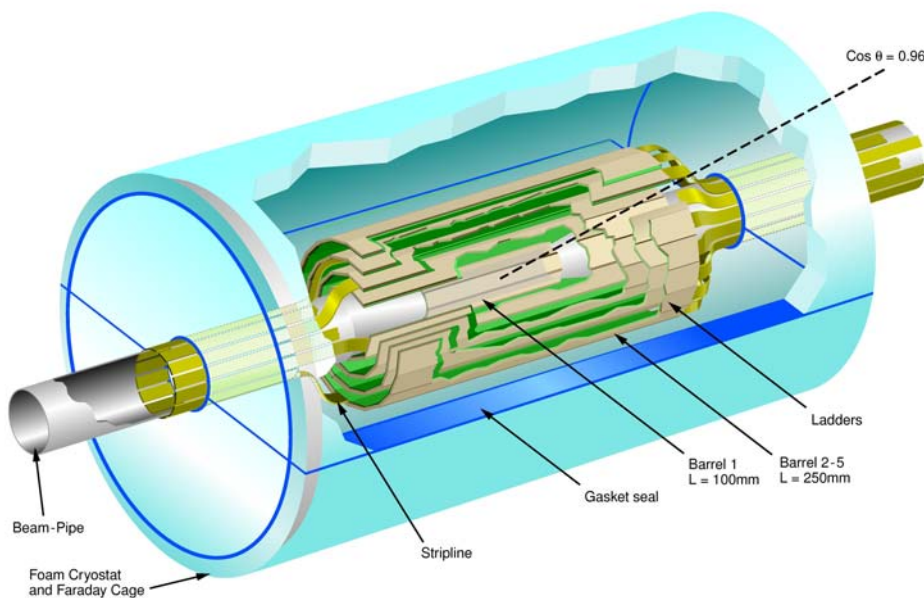


Linear Collider Flavour Identification: Case for Support

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Abstract

The Linear Collider Flavour Identification (LCFI) Collaboration is developing the sensors, electronic systems and mechanical support structures necessary for the construction of a high performance vertex detector at the e^+e^- International Linear Collider (ILC) and investigating the contribution such a vertex detector can make to the physics accessible at the ILC. The collaboration's goal is to produce and test, in five years time, full-scale sensors with the accompanying electronics, support and cooling systems necessary for application at the ILC. These must allow polar angle coverage in the range $|\cos \theta| < 0.96$, readout or signal storage within $50 \mu\text{s}$, and have a material budget of at most $0.1\% X_0$ for normally incident particles, providing an impact parameter resolution of $\leq 5 \mu\text{m}$ for tracks with momentum as low as $1 \text{ GeV}/c$. The sensor development will build on the collaboration's expertise with column-parallel CCDs and will include devices with in-pixel data storage. Readout circuits for these sensors will be designed with on-chip clustering and data sparsification algorithms. Studies of materials allowing the construction of extremely low mass supports for these sensors will be undertaken in conjunction with studies of the mechanical design of the vertex detector. The collaboration's flavour tagging and heavy flavour charge identification investigations will be extended both to optimise the vertex detector design and to maximise the physics potential of the ILC.

1	LCFI: INTRODUCTION AND SCIENTIFIC GOALS	3
1.1	EXECUTIVE SUMMARY	3
1.2	INTRODUCTION.....	3
1.3	FLAVOUR IDENTIFICATION AT THE ILC	4
1.4	THE ILC AND VERTEX DETECTOR DESIGN.....	5
1.5	THE LCFI PROGRAMME	6
1.6	SUMMARY	9
2	LCFI: WORK PACKAGES AND TECHNICAL DESCRIPTION	9
2.1	WORK PACKAGE 1: SIMULATION AND PHYSICS	9
2.1.1	<i>Optimising the vertex detector.....</i>	11
2.1.2	<i>From MIPS to Physics - Tasks.....</i>	12
2.2	WORK PACKAGE 2 – SENSOR DEVELOPMENT	16
2.2.1	<i>Readout options and sensor types.....</i>	17
2.2.2	<i>Development of Column Parallel CCD Sensors.....</i>	17
2.2.3	<i>Development of Storage Sensors</i>	19
2.2.4	<i>Concluding Remarks on CPCCD and Storage Sensors.....</i>	26
2.3	WORK PACKAGE 3: READOUT AND DRIVE ELECTRONICS	26
2.3.2	<i>Development of readout ASICs.....</i>	28
2.3.3	<i>Development of driver ASICs.....</i>	30
2.4	WORK PACKAGE 4: EXTERNAL ELECTRONICS.....	31
2.4.1	<i>CPCCD electronics</i>	31
2.4.2	<i>Storage Sensor Electronics.....</i>	34
2.4.3	<i>Data acquisition and control system.....</i>	34
2.4.4	<i>Additional electronics for beam tests.....</i>	35
2.5	WORK PACKAGE 5: INTEGRATION AND TESTING.....	35
2.5.1	<i>Current status</i>	36
2.5.2	<i>Future tests of CPCCD and Storage Sensors</i>	38
2.6	WORK PACKAGE 6: VERTEX DETECTOR MECHANICAL STUDIES.....	41
2.6.1	<i>Detector Layer Support Technologies</i>	41
2.6.2	<i>Detector Layer Production Methods</i>	44
2.6.3	<i>Vertex Detector Global Design.....</i>	45
2.6.4	<i>Cooling and Thermal Studies.....</i>	46
2.7	WORK PACKAGE 7: TEST-BEAM AND EMI STUDIES	46
2.7.1	<i>EMI Test-Beams</i>	47
2.7.2	<i>Prototype Ladders in Test-Beams</i>	49
2.8	WORK PACKAGE 8: FINANCIAL AND MANAGEMENT	49

1 LCFI: Introduction and Scientific Goals

1.1 Executive Summary

In this proposal, the Linear Collider Flavour Identification (LCFI) Collaboration is requesting funding for a continuation and an expansion of its programme, with the goal of developing the vertex detector sensors and modules to the point at which the functioning of a full-scale prototype module can be demonstrated in a test-beam. In the five year time span of this proposal, LCFI will be bridging the gap between the pure R&D efforts of the collaboration to date with the need to have a demonstrated pre-production module for the International Linear Collider (ILC) by 2010. The results of our tests will be instrumental in determining which devices are used at the ILC. The objective of the LCFI group is to ensure that, at the end of this programme, the sensors it has developed will be those chosen for the ILC and that it will be in a position to lead the construction and commissioning of the vertex detector. This will give UK physicists the opportunity to lead physics analysis at the ILC, focussing on the many measurements in which the identification of the flavour and charge of quarks is crucial.

Highly pixellated sensor elements for the vertex detector are one of the keys to unlocking the physics potential of the International Linear Collider. The unique needs of the ILC lead to highly segmented detector elements of extremely low mass and moderate radiation tolerance. This is as-yet uncharted territory for charged particle detection, and one that pushes the current technology to new areas in the phase space of sensor development. The sensors that will be deployed for the ILC vertex detector are thus unlike any being used in the sciences, and must satisfy an extremely challenging set of requirements. These devices also have a number of interesting commercial spin-offs and have generated interest in the biological sciences.

One of the strengths of the LCFI programme has been the group's unique combination of studies of sensors, of support structures for those sensors and overall vertex detector design, of flavour identification algorithms and of the physics that can be performed using this detector at the ILC. The Collaboration proposes to continue and strengthen aspects of this approach in the future.

1.2 Introduction

Our current understanding of the fundamental interactions of nature is encapsulated in the Standard Model (SM) of Particle Physics. Despite its many successes, it is clear that this model is not complete. It does not provide an explanation for the observed number of generations of quarks and leptons, nor does it account for the relative strengths of the strong and electroweak interactions. New experimental data are needed to determine which, if any, of the many proposed extensions of this theory are able to provide a more complete description of nature. These data will be provided both by the Large Hadron Collider (LHC), now under construction at CERN (which will collide protons with protons at a centre-of-mass energy of 14 TeV) and by the International Linear Collider (ILC), which will collide electrons with positrons at a centre-of-mass energy ranging from 90 GeV to 1 TeV.

An important step towards the realisation of the ILC was taken in 2004, when the International Technology Review Panel recommended that superconducting RF technology be used for the acceleration of the electrons and positrons, rather than the normal conducting alternative. This recommendation was accepted by the American, Asian and European Particle Physics laboratories which are working together to construct the ILC, opening the door to experimentation at this collider from the middle of the next decade. The LHC is scheduled to start operation in 2007 and this timescale, along with the desire for concurrent running of the ILC, drives an ILC schedule where construction starts before the end of the decade and it is operational in 2015-2017. We therefore need to be ready with detector technical designs in only a few years and with prototype modules by the end of the decade.

The ILC and the LHC together will address some of the outstanding fundamental problems in physics. They are likely to provide data on the mechanism through which particles acquire their mass, may reveal new layers in the structure of space-time and may clarify the nature of Dark Matter. Although

they address similar questions, the information provided by the two machines is very different. While the high collision energy of the LHC gives it a large mass reach, the clean collision environment of the ILC, the known collision energy and the availability of polarised beams make it the ideal machine for precision measurements. Detailed studies of the properties of particles discovered at the LHC, or the ILC, thus become possible. The complementary nature of the LHC and the ILC has persuaded the international community that the ILC must be the next major Particle Physics project and that it should operate in parallel with the LHC. Historically, the CERN and Fermilab proton anti-proton colliders, the SppS and the TeVatron, respectively, and the Large Electron Positron collider (LEP) have demonstrated how powerful this synergy can be.

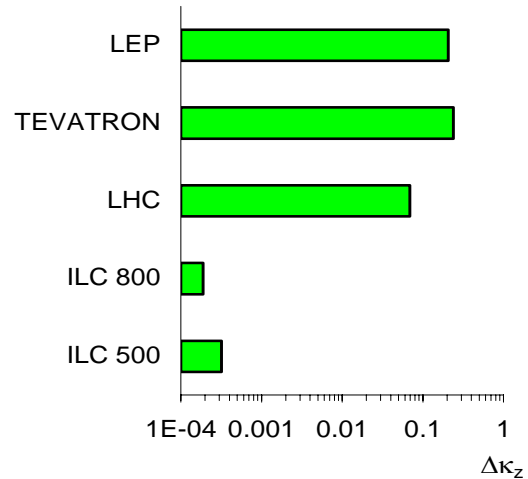


Figure 1.1 Precision of measurements of the tri-linear WWZ coupling ($\Delta\kappa_Z$) at the LHC and ILC (at two centre-of-mass energies 500 and 800 GeV). Note the logarithmic scale.

Two examples illustrate the contribution the ILC can make to our understanding of physics. The first is in the measurement of parameters of the SM: Figure 1.1 shows the precision with which deviations from the tri-linear WWZ coupling expected in the SM, $\Delta\kappa_Z$, can be measured at the LHC and the ILC, while Figure 1.2 shows the precision that can be obtained on the top Yukawa coupling. In both cases, the ILC is seen to provide significant information over and above that which can be obtained at the LHC. Arguments such as these have convinced the UK Particle Physics community that it should invest in the construction of the ILC. PPARC has funded major new initiatives in accelerator science in the Universities and through CCLRC to this end. The aim is that this research and development will allow UK industry to provide high technology components for the ILC to the value of £200M to £300M, the level necessary to ensure a key rôle for the UK in the linear collider project. Similarly, UK investment in the development of the detector technologies necessary for the ILC is crucial to ensure firstly that the collider is fully exploited and secondly that UK physicists are able to play a leading role in experimentation at the ILC.

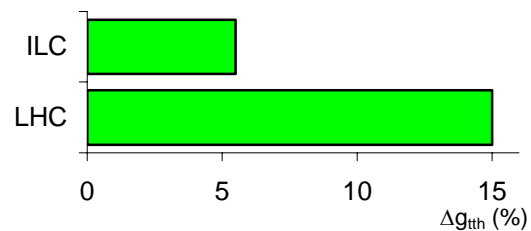


Figure 1.2 Measurement precision of the top Yukawa coupling at the LHC and ILC ($\sqrt{s} = 800$ GeV).

1.3 Flavour identification at the ILC

The two physics examples above can be used to illustrate a further point of interest: both measurements can be greatly enhanced by the identification of the flavour and charge of the heavy c and b quarks produced in the electron-positron collision events at the ILC. As the cross sections for the processes that must be measured in these and other cases are small, the flavour identification must be efficient. Even at the ILC, the backgrounds are significant, so high purity must also be achieved. The only way this can be done is via the measurement of the distance travelled by the b and c quarks between their production and decay. For these decays, the impact parameters of the decay products are typically of the order of a few 100 μm . This requires several space points on the tracks of the b and c decay products be measured with a precision of better than 5 μm within a few centimetres of the production vertex and that this be done with minimal disturbance of the flight paths of those decay particles. The tracking chamber (vertex detector) necessary to accomplish this measurement must thus

perform significantly better than even the best such detector constructed to date, the VXD3¹ of the SLAC Large Detector (SLD) Collaboration which used Charge-Coupled Devices (CCDs) that were designed and manufactured in the UK.

The crucial rôle that heavy flavour identification will play in the physics of the ILC was recognised by the Linear Collider Flavour Identification (LCFI) Collaboration in 1998. At this time, the PPESP approved an exploratory LCFI R&D programme on the possibility of constructing a vertex detector for the ILC based on CCDs. In March 2001, the PPESP approved the start-up of a more ambitious R&D programme, with the goal of developing the design for a CCD-based detector and the accompanying sensors for the future e^+e^- linear collider. At this time, it was unclear whether the ILC would use “warm” or “cold” superconducting RF technology. LCFI proposed to develop CCDs that would satisfy the requirements for operation at the warm LC and would represent a significant step on the road towards sensors suitable for the cold machine, which presents a significantly greater challenge in terms of the necessary readout speed. This was pursued through the development of CCDs with column parallel readout in collaboration with the UK company e2v technologies (formerly Marconi Applied Technologies).

1.4 The ILC and Vertex Detector Design

The baseline vertex detector for the ILC, designed by the LCFI collaboration, is illustrated in Figure 1.3. It has been demonstrated by LCFI to be a powerful tool for flavour identification at the ILC and is currently the starting point for international discussions on the physics performance expected from the ILC. The detector consists of five layers of CCDs with $20 \times 20 \mu\text{m}^2$ pixels which provide a point resolution of about $3.5 \mu\text{m}$ in both the ϕ direction transverse to the beam-line and the z direction along the beam-line. The sensors are arranged in concentric “barrels” around the beampipe. The innermost layer is

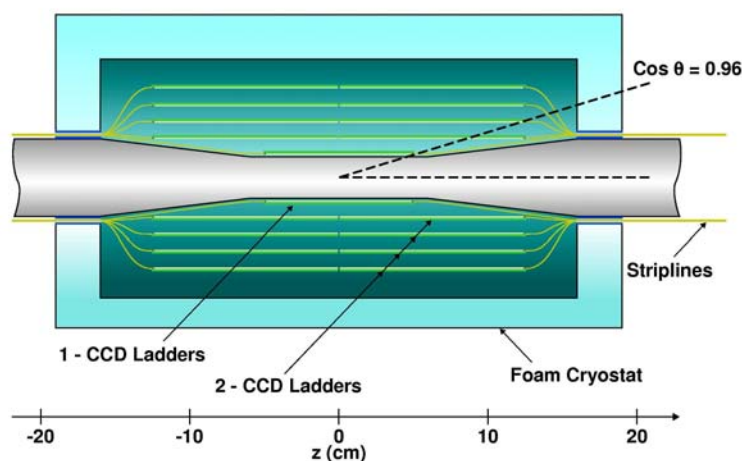


Figure 1.3 The CCD-based vertex detector design developed and studied by the LCFI Collaboration.

at a radius of 1.5 cm and the outermost at 6 cm. In the design shown, the innermost barrel is made up of 8 modules or “ladders”, each of which is composed of a sensor of dimensions $1.3 \times 10 \text{ cm}^2$ with readout and other electronics at both ends. The further layers are constructed using up to 20 ladders, each of which is composed of two sensors of dimensions $2.2 \times 12.5 \text{ cm}^2$ with electronics located at the outer ends only. This design results in a total number of pixels of nearly 10^9 .

Location of the electronics at the extremes of the polar angle θ ensures the amount of material in the central tracking volume is minimised. This is essential as the mean momentum of the charged tracks in heavy quark decays at the ILC is only a few GeV, implying that multiple scattering effects must be minimised. The goal is to produce ladders with a thickness of only $0.1\% X_0$ (c.f. SLD VXD3, $0.4\% X_0$). Minimisation of the material budget also dictates that only gas may be used for cooling the sensors in the sensitive volume of the detector. The sensors must therefore consume at most a few watts of power.

¹ K Abe et al, *Design and performance of the SLD vertex detector: a 307 Mpixel tracking system*, NIM A 400 (1997) 287.

The decision that cold technology be used at the ILC is particularly challenging for the designers of vertex detector sensors. It implies that, at a centre-of-mass energy of $\sqrt{s} = 500 \text{ GeV}$, trains of about 3000 bunches² (or about 5000 at $\sqrt{s} = 1 \text{ TeV}$) will pass through the beampipe within the ILC detector at a frequency of approximately 5 Hz. Within these trains, tightly focused electron and positron bunches collide roughly every 350 nanoseconds (about 150 ns at $\sqrt{s} = 1 \text{ TeV}$). By contrast, the warm RF accelerator technology would have matched better the needs of the vertex detector readout, as its shorter bunch trains provide gaps in which to readout the pixel sensors.

A further challenge at the ILC is illustrated by the experience of the SLD vertex detector, the only vertex detector operated in a linear collider environment to date. It suffered from beam-induced pickup, presumably from the leakage of RF power generated by the wake fields of passing electron and positron bunches. Fortunately at SLD, where the time between bunch crossings was 8 ns, it was possible to wait a few hundred microseconds for the electromagnetic interference (EMI) to die out and the electronics to recover before readout.

1.5 The LCFI Programme

Sensors for the Vertex Detector

The occupancy expected in the inner layers of the vertex detector is such that the detector will have to be read out every 50 μs while the ILC bunch trains are passing through the detector. Since a vertex detector with the properties listed above will have nearly 10^9 pixels, reading out between every bunch crossing is not practical. It is also not necessary, considering the low average occupancy per crossing. There are, therefore, two practical approaches; reading out a few times *during* the long bunch trains, or *storing* the hit information and reading out in the quiet time after the bunch train has passed.

The choice of accelerating technology dictates the beam structure and heavily influences the sensors that can be used for the vertex detector. In the case of the superconducting RF technology chosen for the ILC, the choice of readout strategy is not obvious. The long bunch trains do not provide a natural time in which to read out the detector, and so a storage approach becomes an important alternative. Since the optimal readout approach is not yet clear, LCFI think it is important to investigate the option of storing the information in addition to the baseline program.

If it emerges that the best strategy is to read out the vertex detector multiple times *during* the passing of a bunch train, the current sensor development path of LCFI provides an excellent solution. This development path is primarily concentrating on the development of Charge Coupled Devices (CCDs). These were used in the vertex detector of the SLD experiment, the highest performance vertex detector yet constructed and that closest to the specifications needed for the ILC. Some of the criteria for the ILC vertex detector were already satisfied by sensors used in this device, for example hit resolutions of 3.5 μm were achieved. Improvements are needed in other respects, however. The readout speeds achieved at SLD were orders of magnitude lower than those required and the material budget, while the best of any vertex detector to date, was still significantly above the target for the ILC.

LCFI has made significant progress towards the goal of high readout speed through the development of a column parallel CCD (CPCCD). These are orders of magnitude faster than previous scientific CCDs and have the potential to satisfy the speed requirements of the ILC while presenting very little material to traversing particles. Further development remains to be done to ensure that (a) the required sensor size can be read out at sufficiently high speeds, and (b) that power consumption of the resulting devices can be sufficiently minimised. Once fabricated, our *current* generation of column parallel CCD, at over 9 cm in active length, will be an excellent attempt at addressing the requisite sensor size. The work outlined in this proposal will concentrate on attaining the necessary readout speed for such large sensors (50 MHz) and in making appropriately miniaturised drive electronics.

² Although the design parameters of the ILC have yet to be finalised, the choice of cold technology implies these will be close to those of the TESLA collider which also proposed to use superconducting cavities.

The second approach, that of *storing* the information in the pixels and reading out this information after the bunch train has passed, has led to exciting and new approaches to pixel sensor development. We are fortunate that the originally parallel work of the LCFI and UK-MAPS Collaborations has generated two variants of a storage sensor that can be brought to full-scale devices in the required time: the Flexible Active Pixel (FAPS) and In-situ Storage Image Sensor (ISIS). They both share a similar readout architecture and control scheme and would be both built in CMOS technology. The main difference between the FAPS and the ISIS lies in the way the information is stored in the pixel. In the FAPS, standard CMOS capacitors are integrated in the pixel and keep a record of the voltage at the photodiode. In the ISIS, CCD-like elements are added to the CMOS pixel to store the charge corresponding to the particle hits. An initial ISIS prototype test structure was included in the recent sensor production run and will be investigated in summer 2005. A prototype FAPS was already demonstrated by the PPARC-supported UK collaboration for MAPS.

There are many advantages to storing the data for readout until after the passage of a bunch train. Both ISIS and FAPS designs result in a much reduced readout speed requirement (few MHz). Given the level of similarity between the readout, significant synergy is envisaged in the data acquisition and testing between the two designs—they both will use much the same testing and data acquisition hardware. Each has the possibility of having the sensor and readout electronics fully integrated onto the same piece of silicon, an approach that is attractive for its elegance, mechanical ease, and potential for low mass especially in the forward regions. The FAPS approach should have high radiation resistance, the ability to be made in a standard stitched optical CMOS process, and warmer operational temperatures compared to that of the traditional CCD, which can lead to reduced mass and less restricted mechanical constraints. The ISIS sensor similarly has many advantages and in particular the storage of the raw charge associated with the hit makes it possible to design-in a higher degree of robustness against electromagnetic interference (EMI), the importance of which is illustrated by the SLD experience.

Balanced against the advantages of each sensor there are challenges to overcome, and risks in their development. The primary challenges for the Column-Parallel CCD development remain the achievement of the necessary speed, the development of appropriately low-mass drive electronics, and the additional constraints of low-temperature operation. These issues, together with the ability to re-focus development for a specific beam structure, have led LCFI to pursue storage sensor options. Here too the sensor choice is not immediately obvious. The ISIS sensors should provide substantial resistance to EMI, but it may prove difficult to incorporate a CCD-like storage register in CMOS, or to transfer out the charge from an irradiated sensor without overlapping polysilicon gates. The FAPS sensors should have the necessary radiation resistance, but may well have lower resistance to EMI given that the charge-to-voltage conversion occurs during the bunch train. LCFI will discontinue development of any sensor type that proves unable to fulfil the needs in the ILC, but given the risk associated with any one option and the substantial overlap in development costs, each will be pursued initially.

While each sensor type has particular advantages that can be exploited, the final choice of sensor is not clear. The column-parallel CCD development is currently well advanced and it is the “default solution” for initial designs of the ILC vertex detector. The two variants of storage sensor (ISIS and FAPS) each add substantial benefits but come with differing strengths. They also come with much similarity in readout and control, and as such they can be pursued with substantial beneficial overlap. This offers the maximum flexibility and mitigates the risk associated with pursuing a single approach.

Simulation of the vertex detector and its physics performance

The Collaboration proposes to further develop the simulation of the vertex detector. In particular, this must be extended to include the effects of the actual performance of the sensors, including the effects of the extremely non-uniform charge deposition resulting from the passage of charged particles, of the magnetic field in which the sensors sit and of the readout and signal processing. The importance of such studies is illustrated by the case of the data sparsification algorithms, which must be “hard-wired” into the readout chip. If these are poorly chosen, the physics performance will suffer excessively from the effects of the possible backgrounds in the sensors. Such effects must thus be

accurately simulated and the results of these studies fed into the design of the readout chips. Simulation studies will therefore guide the further development of the sensors and readout chips, the design of the vertex detector and inform efforts to further improve quark flavour and charge identification algorithms.

The impact of the vertex detector on physics studies at the ILC will continue to be investigated. It is crucial that LCFI is able to respond to proposed changes in the ILC design, providing rapid and authoritative statements, based on detailed Monte Carlo studies, of the impact of modifications to, for example, the beam-pipe radius and therefore the ammunition to resist these if they result in significant loss of physics performance. Further, it is important that information be provided now on the possibilities opened up by the addition of new capabilities to the ILC detector. An example here is the question of particle identification. So far this has been thought to be largely irrelevant at the ILC, but the physics gains arising from identification of the charge of b and c quarks are now becoming apparent due to the work of LCFI. Such charge identification can be enhanced by kaon identification, for example³. The ILC community must thus re-assess this question and input from the physics studies of LCFI is crucial to this effort.

Ancillary electronics

Successful development of the sensors for the vertex detector will require the production of the printed circuit boards and external electronics necessary for their testing. The design of these devices will require expert electronic engineering support. For example, in the case of the CPCCD, these boards must provide drive signals for the CCD at a frequency of 50 MHz and in close proximity to this allow the amplification and readout of signals of only 2000 electrons. Measurements of prototype ladders will require the development of the miniaturised electronics necessary to control the readout of the ladder and capture the sparsified data it produces.

Mechanical studies

Sensors capable of particle tracking at the few micron level are of little value if they cannot be mechanically supported in a structure whose behaviour is understood to a similar or better level of precision. Studies of mechanical support structures for the sensors will continue, but will be extended to include new materials such as carbon foams used in the aerospace industry. Simulations of the dynamics of these systems will also be performed. For example, minimizing the power required by the drive electronics for the CPCCD, and hence the mass of any cooling structures, dictates that the drive be operated only during the ILC bunch train. This is likely to result in temperature fluctuations: the vertex detector will heat during the approximately 1 ms long bunch train then cool down in the 0.2 s between bunch trains. The effects of these fluctuations must be understood at the micron level if the detector is to provide the required precision.

Test-beam measurements and EMI studies

LCFI will need to develop the capability to produce full prototype ladders of a future ILC vertex detector and to test them in a test-beam environment. In addition to this, LCFI proposes to investigate potential EMI problems not only by investigating the sensitivity of the sensors it is developing to EMI and improving their robustness but also by developing an understanding of the likely sources and nature of interference using test-beam measurements. A programme of measurements is foreseen for this purpose at the SLAC final-focus test beam and further measurements could also be made at the TESLA test facility at DESY if needed. These studies will include investigations of the effects of the feed-throughs for beam-position monitors and the like which will be necessary at the ILC.

³ K Abe *et al.*, Direct Measurements of A(b) and A(c) using Vertex/Kaon Charge Tags at SLD, Phys. Rev. Lett. **94**: 091801, 2005 (hep-ex/0410042).

1.6 Summary

There is international agreement that progress in Particle Physics in the next two decades will best be achieved through the construction of a Linear Collider with a centre-of-mass energy ranging between the Z mass and 1 TeV. In this proposal, the Linear Collider Flavour Identification Collaboration presents a coherent programme of research, the goal of which is to ensure that UK physicists are in a position to construct the vertex detector for this facility in 2010. The remainder of this document describes the various aspects of this research programme in detail. Eight “work packages” are defined. These describe:

1. The vertex detector simulation and physics studies that must be undertaken in order to optimise the sensors and vertex detector and guide the designers of the ILC.
2. The design and construction of CPCCD, ISIS and FAPS sensors, all of which have the potential to satisfy the demanding requirements for operation at the ILC although there are significant challenges to overcome in each case.
3. The Application Specific Integrated Circuits that must be designed, produced, and tested for the readout of the sensors.
4. The ancillary electronics needed for the testing of the various sensors in the laboratory and for the test of full scale modules in a test-beam.
5. The programme of tests for the various sensor types, including studies of the achievable readout speed and their radiation hardness.
6. The design of mechanical support structures for the sensor modules and of the overall vertex detector.
7. The establishment of a realistic test environment for sensor operation, and the investigations of possible sources of electromagnetic interference and the sensitivity to this interference.
8. The proposed management structure for the project.

2 LCFI: Work Packages and Technical Description

2.1 Work Package 1: Simulation and Physics

Since its formation in 1998, the LCFI collaboration has naturally focussed its manpower on cutting edge detector issues, with the result that simulation and physics work has been lightly manned. Nevertheless, LCFI provided the entire input on flavour ID to the TESLA TDR⁴. The efficiency/purity plots in Z decays (Figure 2.1) and the mis-tag rates as function of jet energy (Figure 2.2) provided the impetus for many physics studies which firmly established the superior flavour ID capability of the proposed TESLA vertex detector. The possibility for a pure, efficient charm tag in the absence of light-quark background, shown in Figure 2.2, has generated considerable recent interest, since it will be essential for measurements of the polarisation of the top quark. As

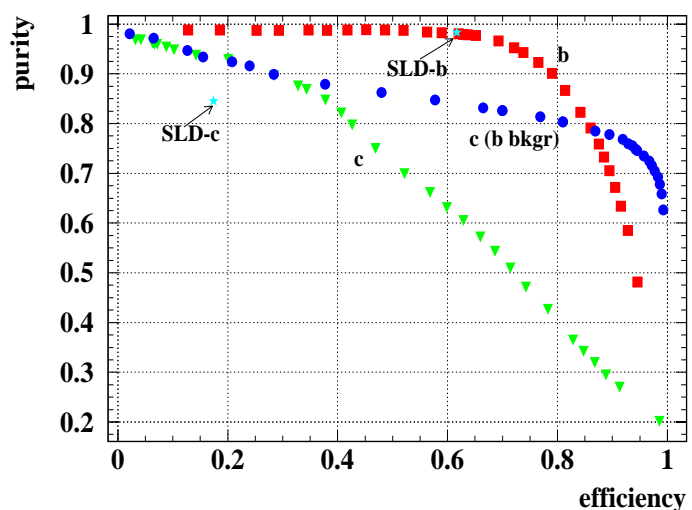


Figure 2.1 Purity versus efficiency for $e^+e^- \rightarrow q\bar{q}$ at $E_{cm} = 91.2$ GeV.

⁴ DESY 2001-011 (2001) IV-54

well as the physics performance, the key detector requirements (small pixels, etc) were established⁵. These studies still represent the state-of-art in terms of the estimated flavour ID capability at ILC. In 2003 an increase in LCFI manpower dedicated to the physics work package allowed some additional jet flavour tagging activity.

After the publication of the TESLA TDR, the linear collider community began to replace the old legacy simulation code with modern object-oriented software. These developments are currently underway in all three regions but are still at a rudimentary level. LCFI therefore took the decision early last year to pursue the urgent studies required to refine the detector design using the robust fast MC program SGV⁶ – the DELPHI experiment’s fast simulation program.

We have recently obtained results on the second major tool beyond flavour tagging that is provided by the vertex detector, namely quark sign-selection for *b* and *c* jets. Figure 2.3 shows, for 100 GeV jets, a preliminary distribution of a related quantity, the reconstructed vertex charge, for charged and neutral B hadrons. For charged *B*s, there is a strong correlation between vertex charge and the quark charge, whereas neutral *B*s will require further analysis, including the 'charge dipole' approach pioneered in SLD.

A detector can never be designed on the basis of a fast MC alone, so a strategy for the 'MIPs to Physics' project has been devised, which forms the basis of the present proposal for this workpackage. Our strategy is to replace the idealised SGV code in stages by a detailed MC simulation of the vertex detector – based on Geant 4 for the propagation of particles and their interactions with the vertex detector materials, and code from SLD, LCFI and international partners to handle the detector-specific aspects. This is a challenging task, but nevertheless vital as the final design of the vertex detector will

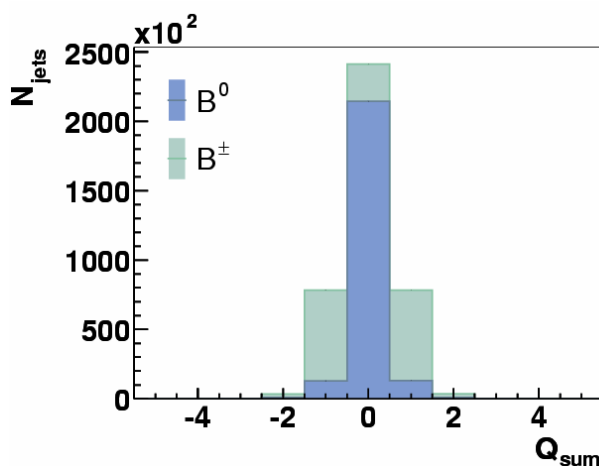


Figure 2.3 : Preliminary vertex charge distributions for 100 GeV b-jets.

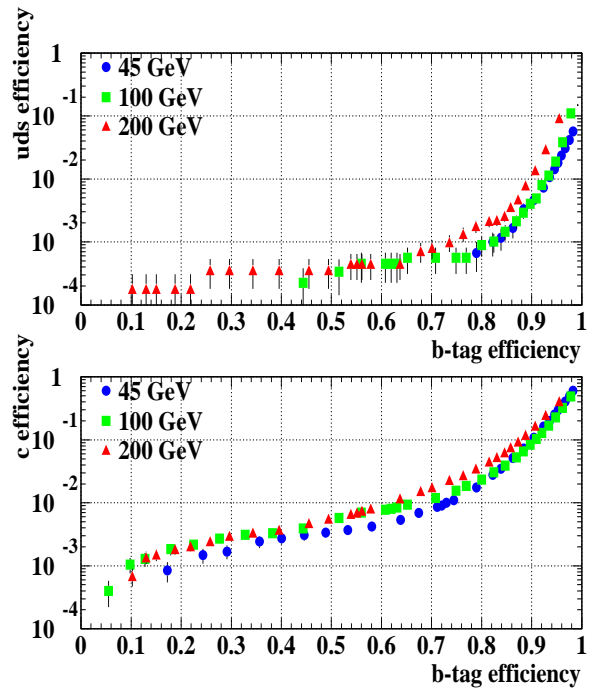


Figure 2.2 Tagging performance for *b* jets of different energies. Efficiencies for 'unwanted' *uds* and charm jets are shown as function of the *b*-tag efficiency.

be based directly on the results of this simulation study. It will be very manpower intensive as detailed detector designs must be implemented, a realistic description of detector performance developed and the necessary reconstruction tools written. Three RAs, starting in October 2005, will be required in order that the MIPs to Physics project will be able to proceed synchronously with the LCFI detector development programme.

The goal of the physics studies is to quantify the dependence of the LC physics on vertex detector design parameters. With the unique experience and expertise we have in the LCFI group we are taking a leading rôle in studying vertex dependent physics in the ILC community. The physics studies form the basis

⁵ S.M .Xella-Hansen, M. Wing, D.J. Jackson, N. de Groot, C.J.S. Damerell, LC-PHSM-2003-0061 (2003)

⁶ <http://berggren.home.cern.ch/berggren/sgv.html>

for the choice of various detector design parameters, such as the number, radii and length of detector layers, the arrangement of barrel staves within the layers, the pixel size and the material budget aimed at.

We are in the process of evaluating these effects, and also need to deal with new issues that arise and have impact on the LC physics. These include the difference between the CPCCD, ISIS and FAPS options and the effects of material at small angles, where the mechanical support and electronics could significantly interfere with the event reconstruction. This and other parameters, e.g. the radius of the innermost layer, which is dependent on the beam-pipe radius, will also have implications for the global ILC detector and the accelerator.

Detailed simulations of the performance of the sensors will influence the development of the readout systems, for example aiding the development of data processing algorithms that are robust against effects such as electronic noise, high track densities in the cores of jets and the increased smearing of clusters at the extremes of the polar angle.

Vertex detector performance will depend on machine backgrounds which affect track reconstruction performance. Collaboration within the UK and at an international level, e.g. with the LC-ABD group studying backgrounds related to the beam-delivery system, will allow us to profit from synergies with neighbouring fields of R&D.

For the coming five years of R&D, we envisage a programme of simulation and physics studies that will take us all the way “from MIPs to physics”. A detailed simulation of the processes that occur when a minimum ionising particle (MIP) traverses the detector will inform the design of the sensors and their readout and provide us with realistic track information in the vertex detector. Based on this description, we will improve our tools for vertexing, flavour-tagging and quark charge reconstruction and extend them to cover the case of neutral heavy flavour hadrons and specific topologies, such as semileptonic decays and events containing neutral kaons and lambdas. It is also likely that use of neutral energy (reconstructed pi-zeroes from the advanced electromagnetic calorimeter) can be used to improve the beauty/charm discrimination. Using these improved tools, studies of physics channels from the fields of Standard Model physics, Higgs physics and Supersymmetry (SUSY) will yield quantitative results on how physics performance depends on the detector design, and how to optimise that design to maximise the physics reach of the ILC.

2.1.1 Optimising the vertex detector

Evaluating and optimising the physics performance of the vertex detector requires that the following topics are addressed:

- overall vertex detector design;
- the material budget;
- simulation of signals from the sensors;
- simulation of data processing and sparsification.

Optimising the overall detector requires choosing the best possible arrangement of the sensors within the detector. Mechanical stability must be ensured, and issues such as the effects of sag, which depends on the length of the detector barrel, considered in the optimisation. The degree of sensor overlap necessary to allow good track based alignment must be determined. Judging from the SLD-experience, a 5-layer long-barrel pixel-based detector will have extremely high track-finding efficiency. However, the performance will of course diminish for very low momentum tracks and at very small polar angles, where the number of hits is reduced. Silicon pixel detectors are extremely reliable, but one cannot completely rule out loss of a sensor, so some redundancy needs to be built into the design. It will therefore be determined whether five layers can provide sufficient redundancy or whether an increase in the number of barrels should be considered. Parameters that are critical for the vertex detector but have wider implications include the beam-pipe radius and the strength of the B-field.

The vertex detector will be affected by the radius and thickness of the beam pipe. These parameters are not independent: increased radius requires increased thickness to resist the forces due to atmospheric pressure on the pipe. The vertex detector will also be affected if shielding requirements dictate that a thin high Z liner must be added to the beam pipe. In turn, the vertex detector itself will affect all systems further away from the interaction point due to the amount of material in the sensors, their support structures, the electronics at the module ends, the electronics in the small angle region, the outer electronics, the support shell to which the modules will be fixed, the cooling system, and the foam cryostat/Faraday cage insulating and shielding the entire system.

Current simulations assume that the sensor signals provide measurement of space points with constant Gaussian errors. In reality, the precision will depend on the charge collection process from the epitaxial layer, which is quite different for the CPCCD and the ISIS and the FAPS. Furthermore, the cluster shapes become elongated, with some degradation in performance, at small polar angles. These effects will be studied by a realistic simulation of the detector signals allowing for non-Gaussian tails on multiple scattering, variable cluster shapes, errors due to noise in the front-end electronics and the digitisation of the data and will be used to optimise parameters such as the pixel size and the thickness of the epitaxial layer.

Any data sparsification system can give rise to loss of data, as memories become filled or clustering algorithms break down. Effects such as high hit densities in the core of jets, background on inner layers from e^+e^- pairs and beam halo tracks, which generate long streaks along the length of the sensor, need to be considered. It is important to develop sparsification algorithms which degrade gracefully in the presence of adverse accelerator operating conditions. These studies will help to guide the design of readout ASICs.

2.1.2 From MIPS to Physics - Tasks

Use of the flexible, well-tested and fast simulation SGV (Simulation a Grande Vitesse) has already allowed us to make progress on vertex and vertex charge reconstruction. Since any fast simulation suffers from simplification, and since it is uncertain at which time another full simulation will reliably provide the functionality needed for our studies, our approach for the MIPS to physics programme is to develop a precise description of the processes in the vertex detector within our Collaboration and to provide an interface to SGV, which will be used to simulate the outer detector. Such an approach is possible because tracking within and outside the vertex detector are independent to a good approximation.

Our programme can thus be divided into three sets of tasks, enumerated in the paragraphs below, each of which will require a similar amount of effort to realise:

2.1.2.1 MIPS to tracks

These tasks comprise development of a detailed description of the processes in our sensors and readout chips, in part based on existing code developed by Su Dong for the SLD Collaboration⁷. The input to this new package will be events from a Monte Carlo program, the output will be track parameters and covariance matrices that can be treated in the same way as the standard SGV variables for the subsequent steps of the simulation and analysis chain. The following tasks are envisaged:

GEANT4 Work (Task 3.1.1)

While SGV assumes Gaussian multiple scattering angular distributions, a precise description will have to take non-Gaussian tails into account. The description of this effect in GEANT4 will be tested and used to arrive at realistic hit positions of tracks on the sensors of the ‘standard geometry’ for the vertex detector. At a later stage, when tools are developed, GEANT4 descriptions of various vertex detector geometries will be developed for comparison and evaluation.

⁷ <http://www.slac.stanford.edu/%7Eesudong/talks/ccdsim-lcpretreat.pdf>

Simulation of charge generation (Task 3.1.2)

A detailed simulation of the charge generation in silicon must be implemented, taking into account the large fluctuations in the numbers of electrons liberated along short sections (1 μm) of the track of a MIP. Such effects must be correctly described if the influence of the magnetic field on the space point measurement made with the sensors is to be accurately simulated.

Simulation of charge collection (Task 3.1.3)

This step depends on the sensor type. For the ISIS and FAPS, two components contribute: charge generated in the depleted region underneath the photogate will be collected fast, charge generated outside that region will be collected slowly (over many nanoseconds) by diffusion. For the CPCCD, the signal charge will all be collected rapidly from a fully depleted, high resistivity epitaxial layer. The ISE-TCAD package, designed for the simulation of silicon devices, will be used to investigate the charge collection process for all these architectures. Three-dimensional look-up tables of the volume of one imaging pixel will then be generated using this information, probably at 1 μm^3 granularity. These tables will be used to determine the pattern of collected signal charge caused by a particular particle traversal. In addition, the effect of the magnetic field will be taken into account in the simulation.

Description of cluster finding and sparsification (Task 3.1.4)

Different cluster finding and sparsification algorithms will be implemented and their effect on the physics assessed. Feedback from these studies will guide the design of future generations of the readout chip.

Track fitting (Task 3.1.5)

Using realistic simulations of vertex detector hits obtained from the previous steps, and the momentum information from the outer tracking detectors provided by SGV, tracks will be fitted to yield track parameters. The Monte Carlo assignment of hits to tracks will be used; track finding, including the effects of background hits will follow at a later stage.

Covariance matrices (Task 3.1.6)

From these fitted tracks, covariance matrices will be obtained, in the same format as used in SGV.

Integration of the MIPs to tracks package into SGV, test and maintenance (Task 3.1.7)

The full chain of routines developed under tasks 1.1 – 1.6 will be tested as a package in combination with SGV. Simulated sparsified raw data (digitised signals in accepted pixels) and fitted track covariance matrices will be written out in LCIO format, for use within and beyond the LCFI programming environment.

2.1.2.2 Tracks to vertex information

This part of the programme will comprise the improvement and extension of higher-level reconstruction tools, such as vertex finding, vertex charge and charge dipole reconstruction and jet flavour-tagging. Since the ILC vertex detector is more precise than previous detectors, the reconstruction algorithms need to be optimised to make use of the improved measurements. Once this has been done, the detector dependence of the reconstructed quantities and of the impact parameter resolution will be studied. In particular, this area will comprise the following tasks:

Update from ZVTOP (Task 3.2.1)

The vertex finder ZVTOP⁸ will be updated to include the so-called “ghost track” algorithm, which takes into account correlations between the positions of the B decay vertex and the subsequent tertiary vertex resulting e.g. from a D meson decay. In addition, special treatment of one-prong vertices is

⁸ D.J.Jackson, *A Topological Vertex Reconstruction Algorithm for Hadronic Jets*, Nucl. Inst. and Meth. **A388**, 247, (1997).

envisaged, which is expected to improve the charm-tagging capability in cases where the light quark background is small⁹.

Use of vertex information to improve jet finding (Task 3.2.2)

In some cases, in particular in multi-jet environments, tracks can clearly point to a vertex contained in a jet other than that to which the track is assigned by the jet-finder. Thus using vertex information can improve the assignment of tracks to jets.

Neural network based flavour-tag and vertex charge reconstruction (Task 3.2.3)

Both flavour-tag and vertex charge reconstruction involve the assignment of tracks to the heavy hadron decay after the ZVTOP code has run. To make optimal use of correlations between the variables that help distinguish whether a track originated from the interaction point or a secondary vertex, a neural network is used. The choice of input variables to the network will need to be reassessed and optimised in parallel with the improvement of the detector description and the other higher level reconstruction tools (tasks 2.1, 2.2).

Extension to neutral B's, e.g. charge dipole (Task 3.2.4)

About 60% of the heavy hadrons in b- and c-quark jets are neutral. For these, the quark charge cannot be inferred from the vertex charge, but requires a dedicated algorithm, such as reconstruction of the charge dipole between the secondary and tertiary vertices, as demonstrated in SLD¹⁰.

Recovery algorithms for special topologies (Task 3.2.5)

The ability to distinguish between jets containing semileptonic heavy hadron decays and purely hadronic jets would allow an improvement in the precision of the jet energy measurement. While energy can be precisely measured for hadronic jets, in semileptonic decays part of the energy is carried away by the neutrino produced. In such cases, estimation of the neutrino energy, extending the procedure used for the p_T -corrected mass, may improve the energy measurement. Identification of leptons will help with beauty/charm jet separation, as well as jet energy determination. Measurements of high-energy neutral pions made in the fine-grained calorimeter may also allow improvement of the determination of the heavy hadron effective mass. Flavour-tagging and vertex charge reconstruction may profit from identification of neutral kaons and lambdas in the vertex detector.

Study of polar angle dependence (Task 3.2.6)

Forward-backward asymmetry measurements depend on the detector performance at the extremes of the polar angle range. The oblique tracks in this region suffer increased multiple scattering, for example, but the hit clusters they produce are also elongated, perhaps resulting in changes in the precision with which the hits are reconstructed. These effects must be quantified and fed into both sensor optimisation studies and investigations of the physics performance of the vertex detector.

Alignment issues (Task 3.2.7)

Requirements in terms of sensor overlap and tolerance for the positions of sensors along the beam direction and perpendicular to it will be evaluated and taken into account in the overall detector design. The effects of misalignments must be investigated and hence the precision with which the position of the sensors must be known evaluated. Alignment procedures can be studied using simulated e^+e^- data and hence the necessary sensor overlap defined.

2.1.2.3 Physics channels

The full vertex detector description (task 1) and on higher level reconstruction tools (task 2) will be used to investigate physics channels sensitive to the vertex detector capabilities. Both studies of known processes, such as top production, and the testing of new physics models which predict a range

⁹ CJS Damerell and DJ Jackson, *Vertex detector technology and jet flavour identification at the future e^+e^- linear collider*, Proc 1996 DPF/DPB Summer Study on High Energy Physics, SLAC Publication, 442 (1997).

¹⁰ TR Wright, *Parity violation in decays of Z bosons into heavy quarks at SLD*, SLAC-R-602 (2002).

of new phenomena depend crucially on the vertex detector performance. The main processes that will be studied are described below, as are the requirements they impose on the vertex reconstruction. The three areas considered are: 3.1) Standard Model studies, 3.2) Higgs physics and 3.3) SUSY and other “beyond the Standard Model” processes. Each of these will require a similar amount of effort.

- **Top events.** The production of $t\bar{t}$ events at the ILC will typically result in a final state containing six jets. Two of these are bottom jets and up to two are charm jets. The reconstruction and identification of these events will rely on the jet flavour tagging and vertex charge reconstruction abilities of the vertex detector both to reduce the combinatorial background and to allow the measurement of the polarisation of the top quark.
- **The Higgs self-coupling.** The Higgs sector is both a central part of the Standard Model and the part that is least well understood. If the Higgs boson is discovered at the LHC, detailed study of Higgs phenomenology at the ILC will be needed in order to better understand the mechanism of electroweak symmetry breaking. One of the central parameters in the model is the Higgs self-coupling, which may be measurable at the ILC through the reconstruction of ZHH events. Since a light Higgs is expected to decay predominantly to bottom quarks, the ZHH events will contain at least four b jets, in a pattern giving with jet-jet masses consistent with the Higgs mass. High performance flavour tagging of all jets in such a multi-jet environment will require optimal reconstruction of the jets over the full momentum and angular range. Vertex charge determination will allow the reduction of the combinatorial background when forming possible jet-jet pairings.
- **Higgs branching fractions.** If the Higgs is light, measurements of ZH events will be crucial for understanding the nature of the Higgs boson. The Standard Model predicts the decay branching fractions of the Higgs as a function of its mass. Any deviation from these predictions will indicate that the Higgs observed is “non-standard”. Of central importance will be a determination of the ratio of the branching fractions $\Gamma(H \rightarrow c\bar{c})/\Gamma(H \rightarrow b\bar{b})$. For example, this ratio is predicted to be smaller than expected in the Standard Model in supersymmetric extensions of the theory¹¹. The full jet flavour tagging apparatus, allowing the separation of b, c and from light flavour jets, will be required for this measurement.
- **SUSY scalar top.** The LCFI group in collaboration with colleagues from DESY has initiated studies of the efficiency with which stop anti-stop production process $e^+e^- \rightarrow t\bar{t} \rightarrow c\tilde{\chi}_1^0\bar{c}\tilde{\chi}_1^0$ can be identified with the vertex detector. The signal for stop production is the production of two charm jets associated with the missing energy carried away by the neutralino ($\tilde{\chi}_1^0$) pair. Signal and background rates have been determined for two different vertex detector inner radii and two different layer thicknesses assuming that there is a large mass difference, Δm , between the scalar top and neutralino mass. Particularly challenging for the vertex detector is the case of small Δm which results in small charged-track multiplicities. This case is well motivated theoretically¹² and is very difficult or impossible to study at the LHC. Work on this channel with the LCFI vertex detector has started in an extended international collaboration, taking full advantage of the available expertise on the expected dominant background from two-photon processes.
- **SUSY CP asymmetries.** The SUSY parameter space includes CP sensitive observables in neutralino production. In the process $e^+e^- \rightarrow \tilde{\chi}_i^0\tilde{\chi}_j^0$ followed by the decays $\tilde{\chi}_i^0 \rightarrow \chi_n^0 Z$ and $Z \rightarrow q\bar{q}$ or $Z \rightarrow l\bar{l}$, it has been shown that the measurable asymmetries are up to six times

¹¹ J Kamoshita, Y Okada and M Tanaka, Determination of the parameters in the MSSM Higgs sector from detailed study of the Higgs properties, Proc. Workshop on physics and experiments with linear colliders, World Scientific (1996)

¹² C. Balazs, M. Carena, C.E.M. Wagner, Phys. Rev. D70, 015007 (2004).

larger for the $Z \rightarrow q\bar{q}$ case than $Z \rightarrow l\bar{l}$ case¹³. Both vertex charge reconstruction and flavour identification are crucial to these measurements.

- **New s-channel resonances.** A number of models predict new resonances, similar to the Z^0 boson, that would be observable through the process $e^+e^- \rightarrow f\bar{f}$. One such model is the “Little Higgs” in which extra gauge bosons are produced in the simultaneous breaking of global and local symmetries. The ability to measure asymmetries for charm and bottom quarks in the final state of such processes using vertex charge will be crucial to the determination of the underlying physics.
- **Higgs parity.** In the Minimal Supersymmetric Standard Model, the CP-even H^0 and CP-odd A^0 Higgs states can in principle be distinguished by reconstructing an acoplanarity angle from the directions of the final decay products in the $Higgs \rightarrow \tau^+\tau^-$ channel. The identification of tau decays from the Higgs in ZH events relies directly on the impact parameter resolution of the vertex detector. Hence the study of the impact parameter performance of the detector, as well as vertex finding, is relevant to the physics capabilities of the detector.
- **The Unexpected.** The above new physics processes provide benchmarks for assessing the potential impact of the vertex detector on measurements that may be made at the ILC. To address the case in which there may be new, unexpected physics that will rely on the precise tracking of the vertex detector, we shall also establish in general terms how much the impact parameter resolution and jet flavour tagging performance of the detector would benefit from improving the current conceptual design.

Work on the physics channels is ongoing and is expected to continue simultaneously with the MIPs to tracks and tracks to vertex tasks.

2.1.2.4 National and international collaboration

We expect that our studies of the physics processes above will benefit from collaboration with the IPPP in Durham. As well as using the SGV framework developed by European groups working on the ILC project, we have established and maintain links with a number of groups around the world. Institutes that have expressed an interest in working on physics studies in association with LCFI include Oregon, SLAC, Fermilab and Yale in the USA and KEK in Japan. We also have collaborative exchanges with DESY-Zeuthen, Nijmegen and Vienna in Europe. It is to be hoped that in due course the various local initiatives will combine in a coordinated worldwide programme of physics studies. A first step towards that goal may be a comparison of results from the different frameworks via the LCIO persistency framework for linear collider detector simulation studies.

2.2 Work Package 2 – Sensor Development

A highly pixellated vertex detector is essential to accessing the physics potential of the International Linear Collider (ILC).^{14,15} The ILC is a machine built for precision measurements, and as such it requires sensors that are at the limits of current technology in terms of segmentation and mass. This is as-yet uncharted territory for charged particle detection, and one that pushes the current efforts to new

¹³ A. Bartl et al, *CP sensitive observables in $e^+e^- \rightarrow \tilde{\chi}_i^0 \tilde{\chi}_j^0$ and neutralino decay into the Z boson*, hep-ph/0402016.

¹⁴ CK Bowdery and CJS Damerell, *Workshop on Physics and Experiments with Linear Colliders*, Waikoloa, Hawaii, World Scientific (1993) 773.

¹⁵ *A vertex detector for the future linear collider*, Stefania Xella Hansen, Nucl. Instr. and Methods A511 (2003) 229 (Proceedings of the VERTEX2002 workshop).

areas in the phase space of sensor development. The sensors for use in the ILC Vertex detector must:¹⁶

1. Allow space-point measurements with a resolution of 5 μm or better.
2. Have a two-track resolution of 40 μm or better.
3. Present at most 0.1% X_0 of material in their active volume to normally incident particles, including all necessary electronics and support structures.
4. Consume at most a few tens of watts of power, allowing the use of a gas cooling system.
5. Cope with operation in a magnetic field of strength up to 5 Tesla.
6. Allow readout or local storage of signals at intervals of 50 μs during the ILC bunch train.
7. Be insensitive to both RF radiation generated by the ILC beams and noise produced by other components of the ILC detector.
8. Withstand a radiation dose of 20 krad per annum resulting from pair production background.
9. Survive an annual dose of 10^9 1 MeV equivalent neutrons per square centimetre originating from the beam and beamstrahlung dumps.

The first four requirements above are driven by the need to make high precision measurements of low momentum tracks within dense jets in the ILC detector, this being necessary to achieve efficient flavour identification, whereas the latter requirements arise from the environment in which the sensors must operate.¹⁷ Currently, there are no sensors which meet all these criteria, and thus the sensors that will be deployed for the ILC vertex detector are unlike any being used in the sciences.

2.2.1 Readout options and sensor types

As discussed in the Introduction, the beam structure of the ILC has significant implications for the design and readout of the detectors. The choice of superconducting radio frequency (RF) as the accelerator technology leads to very long bunch trains (~ 3000 bunches of electrons and positrons). Given that the vertex detector described above will have nearly 10^9 pixels, reading out between every bunch crossing is not practical. It is also not required, as the average occupancy per bunch crossing is low. The occupancy is not negligible, however, and tracking performance may start to suffer after about 150 bunch crossings, forcing readout of the sensors every 50 μs . There are, therefore, two approaches that can be taken. The pixels can be read out several times *during* the bunch train, or the hit information can be *stored* and read out in the quiet time after the bunch train has passed. Following the technology decision, the LCFI Collaboration started to develop, in addition to CCDs^{18,19}, sensors which *store* signals from several bunch crossings locally within the pixels, and read out these signals only after the bunch train has passed. The main objectives of Work Package 2 are thus; (1) the development of Column-Parallel CCD sensors, and (2) the development of Storage sensors.

2.2.2 Development of Column Parallel CCD Sensors

2.2.2.1 Current Status – CPC1 and CPC2

Together with e2v technologies Ltd. (UK), LCFI has designed, produced and tested its first column parallel CCD²⁰, the CPC1. The CPC1 is a two-phase CCD with a pixel size of $20 \times 20 \mu\text{m}^2$ and with 400 pixels in the vertical and 750 in the horizontal direction. The CPC1 is optimised for low voltage operation and features two charge transport regions. Various readout modes are also provided. Sections of each of the two halves of the CCD are equipped with two stage source followers, further sections with single stage source followers and the remainder with pads allowing direct readout of the

¹⁶ See, for example, http://tesla.desy.de/new_pages/TDR_CD/PartIV/detect.html

¹⁷ N. de Groot, *From pixels to physics*, Nucl. Instr. and Methods A501 (2003) 229 (Proceedings of the VERTEX 2001 workshop).

¹⁸ C. J. S. Damerell, *A CCD-based vertex detector for the future e^+e^- linear collider*, Nucl. Instr. and Methods A512 (2003) 289 (Proceedings of the 9th European Symposium on Semiconductor Detectors).

¹⁹ C.J.S. Damerell, *CCD-based vertex detectors*, (2005) Nucl. Instr. and Methods (2005), to be published.

²⁰ See <http://hepwww.rl.ac.uk/lcfi/public/stefanov4ecfadesy.ppt> for a report.

charge accumulated in the CCD (see Figure 2.4). The one-stage source followers and charge readout are on a $20\mu\text{m}$ pitch, allowing either wire- or bump-bonding to the column parallel CCD readout chip, the CPR1, which is discussed in Work Package 3, or wire-bonding to other external electronics. The two-stage source followers allow wire bonding of a limited number of columns to other external electronics for test purposes.

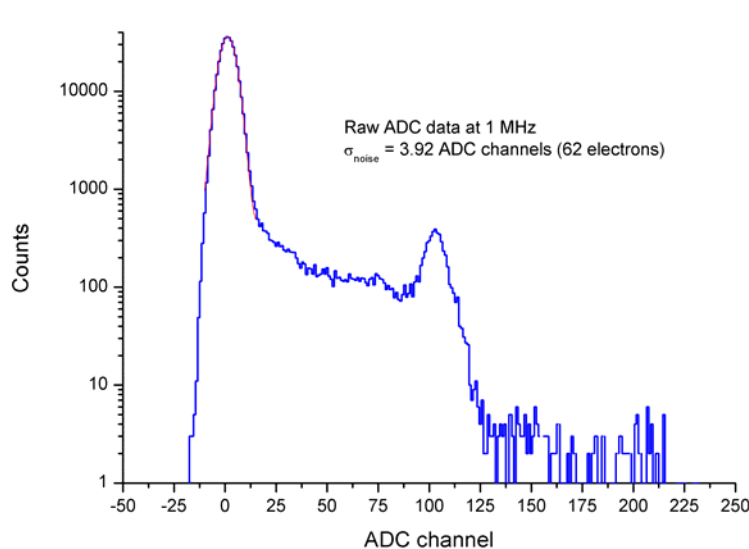


Figure 2.5 Signal due to ^{55}Fe x-rays in CPC1.

The CPC1 chips obtained from e2v technologies were tested and found to function superbly, as is illustrated in Figure 2.5 which shows the signal produced by X-rays from a ^{55}Fe source (primarily 5.9 keV). The readout in this example was driven at the design speed of 1 MHz, but maximum speeds of 25 MHz were achieved with this device. A further success was the reduction of the clock potentials necessary to achieve efficient charge-transfer from values around 10 V peak-to-peak which are typical for CCDs, to a minimum of 1.9 V, with the concomitant decrease in power dissipation in the clock drivers.

Following the testing of CPC1, a second column parallel CCD, CPC2 was designed and is currently under construction by e2v. The CPC2 design includes: (1) field-enhanced and standard charge transport sections, to study methods of faster readout, (2) a low-dose implant to study the correlation between efficient charge-transfer and low clock potentials, (3) a range of epitaxial layers to study the problems of charge collection at high speeds, and (4) high speed clock signal propagation enabled by a “busline-free” architecture, devised at RAL. In the latter, drive signals are distributed using two metal layers that cover the entire imaging area of the CCD, separated by an insulating polyimide layer. All these features will require extensive testing and evaluation, presented in Work Package 5.

A range of sensors will be delivered, including sensors with image areas of $13\times 15\text{ mm}^2$ and $53\times 15\text{ mm}^2$. These chips are designed to be clocked at up to 50 MHz. A large area stitched CPC2 will also be delivered, with an imaging area of size $9.2\times 1.5\text{ mm}^2$ and total dimensions of $10.5\times 1.7\text{ mm}^2$. This sensor is nearly the size required for the outer layers of the ILC vertex detector, and as such it will allow investigation of the problems associated with the production of full-scale sensors, such as the propagation of the clock signals across the full image area. The CPC2 will also be used to investigate the sensitivity of the CPCCD and its readout to electromagnetic interference (EMI). These studies are described in more detail in Work Package 7.

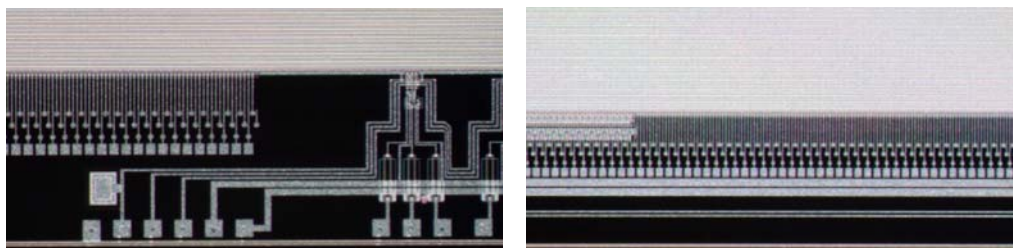


Figure 2.4 CPC1 readout options: left photograph, from left to right, direct connections allowing charge readout and two-stage source followers; right photograph, from left to right, one-stage source followers and direct connection, both on a pitch of 20 micrometers.

2.2.2.2 CPCCD Sensor Development – Tasks and Plans

Following on the test results of the CPC2 sensors (Work Package 5), three development cycles are envisaged for the duration of the five-year proposal.

2.2.2.2.1 CPC Test Structure Studies (Task 2.1: 2005 to 2006)

The design of drive circuitry that can steer (“clock”) the charge-transfer over the full imaging area of the CPCCD, and do so without adding excessive material, remains one of the challenges for LCFI. This requires development of the drive itself, but also the minimisation of the load with which this drive must cope. A series of test structures will be devoted to achieving this goal. The lowest possible drive voltages will be achieved by studying a series of chips with a range of dimensions of the stepped nitride insulator under the poly-silicon gates in one case and a range of low level implants under the gates in another. Reduction of the load caused by the inter-gate capacitance will be achieved by minimising the thickness of the poly-silicon gates. A further reduction in the capacitive load can be achieved by increasing as much as possible the thickness of the polyimide layer between the metal bus layers. LCFI has been offered the opportunity by e2v to produce the chips necessary for these studies as “passenger” devices on wafers that are being processed for other purposes, reducing costs considerably.

2.2.2.2.2 CPC3 (Task 2.2: 2007 to 2008)

The CPC3 sensor will be the first large scale CPCCD designed to run at 50 MHz. It will use the busline-free design pioneered on the CPC2. The depletion depth, the construction of the gates and the choice of field-enhanced or standard charge-transfer regions will all depend on the results of the evaluation of CPC2 and the subsequent test devices. These sensors may also be the first onto which the driver is bump-bonded between the imaging area and the readout ASIC. This arrangement will be essential to avoid the loss of the drive signal that would result if it had to be taken via buslines past the readout chip.

The CPC3 allows the investigation of the problems associated with scaling up the fast CPCCD to full size ($12.5 \times 2.2 \text{ cm}^2$) and with constructing detector modules (“ladders”) using these sensors. Problems can thus be identified and solved before the production of the full scale sensors for the test-beam studies on which the choice of the sensor technology for the vertex detector of the ILC will be based.

2.2.2.2.3 CPC4 (Task 2.3: 2008 to 2009)

The CPC4 sensors will have dimensions of $10.0 \times 1.3 \text{ cm}^2$ or $12.5 \times 2.2 \text{ cm}^2$ as is currently envisaged for the inner and the outer layers of the vertex detector, respectively. Clock potentials will be in the range 1 to 2 volts peak-to-peak, with the integrity of the signals being ensured by the use of “bus-line free” clock distribution. The CPC4 sensors will also have a fully depleted epitaxial layer to ensure that charge collection is possible in a time compatible with the readout speed of 50 MHz. Test-beam studies of these and other full-scale devices will determine the sensor technology for the vertex detector of the ILC.

2.2.3 Development of Storage Sensors

2.2.3.1 In-situ Storage Image Sensor

The principle underlying this sensor is illustrated in Figure 2.6. Charge liberated by particles passing through the sensor is collected on the photogate in each pixel and then transferred to a CCD register within the pixel. It is stored in this register until the bunch train has passed, at which point readout is started. The timescale for the readout is relaxed, allowing relatively long shaping times and hence accurate conversion of the charge to voltage, possibly with concomitant improvements in the hit precision. Also, as the number of charge-transfers is reduced by a large factor, the effect of a small charge-transfer inefficiency and hence the sensitivity to radiation damage is sharply reduced. Further, operation at higher temperature becomes possible.

In addition to the advantages listed above, the ISIS architecture represents the technology that can be made the most robust against electromagnetic interference (EMI). This challenge to vertex detection is best illustrated by the experience of the SLD. It suffered from beam-induced pickup, presumably from the leakage of RF power generated by the wake fields of passing electron and positron bunches. Fortunately at SLD, where the time between bunch crossings was 8 ms, it was possible to wait a few hundred microseconds for the electromagnetic interference (EMI) to die out and the electronics to recover before readout. EMI induced noise can be particularly problematic for sensors where charge-to-voltage conversion of the signal occurs during the bunch train. The use of Correlated Double Sampling should help suppress noise, especially in sensors with a short time between successive samples (i.e. 20 ns in the case of CPCCD). For the ISIS however, we are storing the *raw charge* associated with the charged particle passage and reading it out only after the electrically active period during the bunch train passage. As such the ISIS has the potential to be the most robust against EMI.

Various ISIS structures are conceivable²¹. Those described in the following require the combination of features typically found at CMOS and CCD foundries, restricting the number of manufacturers able to produce the devices, but opening up the possibility that the sensor and readout chip be incorporated on one silicon wafer, potentially reducing the amount of material at the ends of the ladders and providing improved vertex detector performance in the forward region. As this type of sensor has not yet been investigated for applications in particle physics or astronomy, significant research and development will be necessary before practicable devices are achieved.

2.2.3.1.1 Linear and Circular In-situ Storage Image Sensors

One realisation of the ISIS architecture is to have a linear charge storage register which is driven as a 3- or 4-phase CCD within each pixel. Figure 2.6 shows two ways that this may be achieved. Design A requires a high energy p implant with small apertures through which the signal charge is collected. Design B relies on punchthrough of the relatively lightly doped p+ well during collection of the signal charge. This may require excessive gate voltage, given the requirement that the well should not be punched through elsewhere (e.g. in any part of the output circuit). First simulations of the linear ISIS

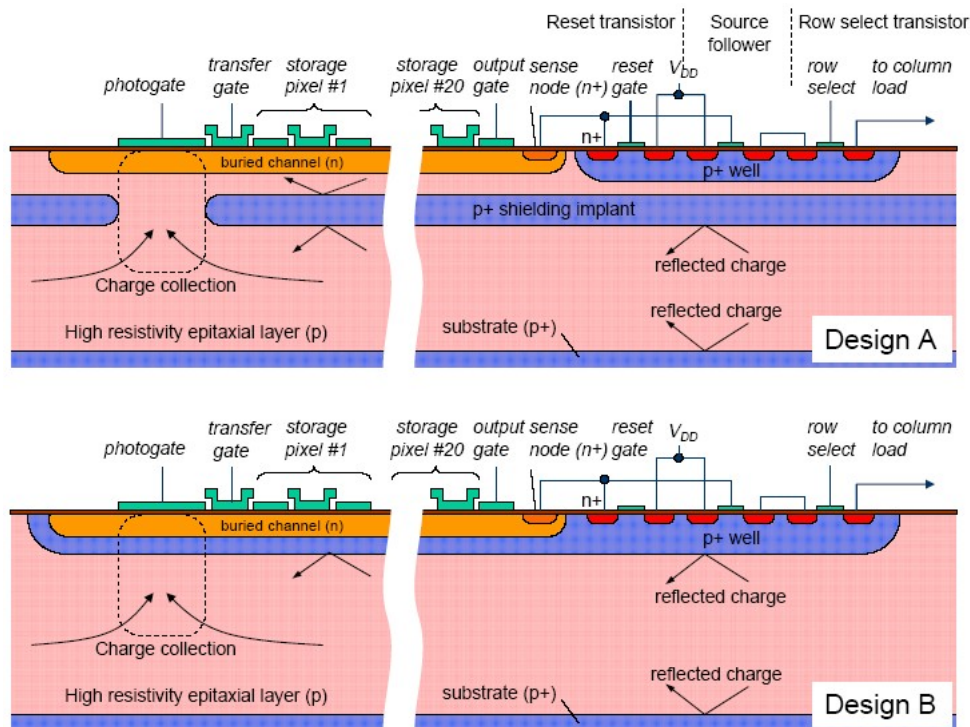


Figure 2.6 Two designs for the linear in-situ storage image sensor.

have been performed using the ISE-TCAD software and suggest there are no fundamental problems with this architecture.

Perhaps even more intriguing is a circular ISIS structure, as illustrated in Figure 2.7. In this case, instead of having a linear register of length 20 within each pixel of the ISIS, there are 20 independent storage gates arranged around the central photogate. Charge collected on the photogate is transferred to each register in turn during the bunch train, and readout is initiated only once the bunch train has passed. Readout is performed by transferring the charge from each of the storage registers in turn back to the photogate and finally to the read out node. This further reduces the number of transfers required by each charge packet, potentially increasing the radiation tolerance of the device and the temperature at which it can be operated.

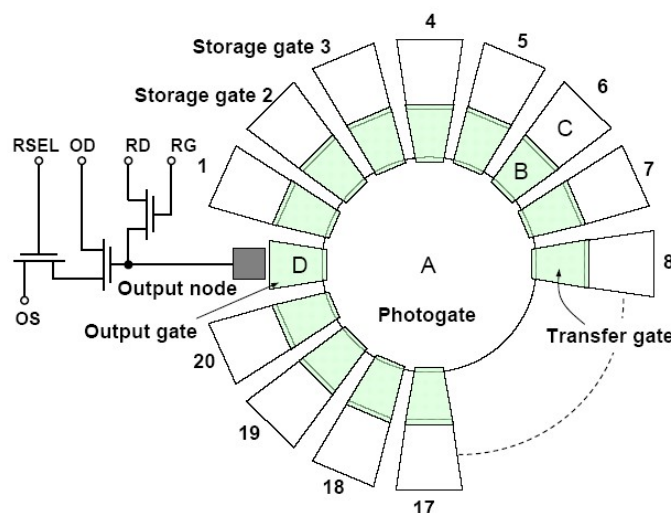


Figure 2.7 Circular ISIS layout. Charge generated at the photogate (A) is moved via a transfer gate (B) to a storage gate (C). Upon readout of the stored charge in cell seven, charge is transferred back from C to B to A, and finally via output gate (D) to the output node.

A possible problem with the circular ISIS architecture is the large difference in size of the photo and transfer gates. In order to check that this does not result in inefficient charge-transfer, the circular ISIS was simulated using the ISE-TCAD package. The results show that high efficiency charge-transfer can be achieved, but that the time this takes is about 150 ns.

2.2.3.1.2 Current Status – ISIS1

The ISIS1 is being made at e2v technologies and will be delivered in July, 2005. It has a structure similar to Design B in Figure 2.6 and uses the punchthrough effect to extend the depletion under the photogate into the epitaxial layer beneath the p-well. The device is an array of 16×16 pixels on a $40 \mu\text{m}$ (H) \times $160 \mu\text{m}$ (V) pitch, the construction being limited by the single level metal and feature size available at e2v. Each ISIS1 cell contains a 3-phase CCD with 5 pixels, a reset transistor, a source follower with an active load and a row select transistor. Each column is buffered by a second source follower working with an external load. The potential required to achieve punchthrough is around 15 to 20 V. There is no on-chip logic and the analogue switches that clock and enable selected rows and all other required signals are provided by external electronics. Testing of this device will be described in Work Package 5.

2.2.3.1.3 ISIS Sensor development – Tasks and Plans

The first ISIS structure is being constructed by e2v technologies and it should demonstrate the viability of the ISIS concept. In parallel with the tests of this device, simulations of the performance of various ISIS designs will be made. These tests and simulations will inform the design process for the next generation of ISIS chips. In all, three generations of ISIS sensors are required in the five year duration of this proposal.

LCFI has so far identified three companies that can make the ISIS sensors. The most promising of these companies is Jazz Semiconductor (formerly part of Rockwell) which is based in California and works with a wide range of deep sub-micron CMOS processes, can perform the deep implantation necessary for the ISIS and also can process a range of epitaxial layers including thicknesses and

²¹ See, for example, http://www.linearcollider.ca/lcws05/h/LCWS05_VTX_STefanov.pdf

resistivities suitable for the ISIS. The one desirable feature that is not offered by Jazz Semiconductor is the ability to produce overlapping polysilicon layers, often used in the manufacture of CCDs to ensure inter-pixel charge-transfer inefficiencies that are below the 10^{-6} level. However, many CCDs are constructed with non-overlapping gates, and achieve high transfer efficiencies. These structures may be less radiation hard than CCDs with overlapping polysilicon gates, and this will need to be investigated carefully.

2.2.3.1.4 ISIS2 (Task 2.4: 2005 to 2006)

The second-generation ISIS devices will be made with CMOS processing, which is a major task involving the design of a new type of semiconductor device. One particular challenge is the implementation of a buried channel CCD structure compatible with the voltages available in CMOS devices (3.3 V or lower), which requires extensive device simulations. The work done so far gives us confidence that this can be achieved. The design phase will proceed in close interaction with experienced CCD designers from e2v technologies and an ASIC designer at RAL. The most promising design for the CMOS process is Design A shown in Figure 2.6. Because the ISIS requires process modifications, the interaction with the process engineers and developers at the semiconductor foundry at all stages of the design will be crucial.

If we choose Jazz Semiconductor for the manufacture, the ISIS2 will be made with single level non-overlapping polysilicon gates. ISIS2 may need a dual level SiO₂ layer, thicker under the CCD gates and with standard thickness for the digital transistors. This is possible using the process at Jazz Semiconductor. The other modification needed to the standard CMOS process is the buried deep p+ implant for shielding the CCD structure from parasitic charge collection. The required implant energy is 1-2 MeV, which is available at Jazz.

At least 4 different linear and circular ISIS devices will be designed and implemented to test their functionality and optimise various parameters. Additionally, at least 2 arrays of linear and circular ISIS devices will be designed as a step towards ISIS3. We will aim to achieve a pixel size of $20 \times 20 \mu\text{m}^2$ in ISIS2.

2.2.3.1.5 ISIS3 (Task 2.5: 2007 to 2008)

The ISIS3 will be constructed using the parameter set determined from the studies of the ISIS2 as a baseline. Based on the test results of ISIS2, the most promising ISIS architectures will be selected for the ISIS3. In all probability, the ISIS2 studies will have allowed LCFI to decide whether to pursue the linear or circular architecture, and only the preferred option will be further studied. For ISIS3, several arrays will be constructed, at least one of which will be designed for bump-bonding to a dedicated readout chip. The largest device will probably be $20 \times 20 \text{mm}^2$ in size with $20 \times 20 \mu\text{m}^2$ pixels. The logic for row selection and clocking will be implemented on the chip. Some test devices may be made with sub-reticle seamless stitching to verify the capabilities of the foundry and prepare for ISIS4. The process modifications for ISIS3 will be mainly to fine tune the design after the successful manufacture of ISIS2 and it is expected that little further process development work will be necessary. One possible exception is that process development may be required if the radiation damage studies show that overlapping gates are mandatory.

2.2.3.1.6 ISIS4 (Task 2.6: 2008 to 2009)

The ISIS4 will be a fully stitched large area sensor with size suitable for construction of prototype detector ladders. The design will use the information learned from the tests of ISIS3 and should not require further modifications to the CMOS process. Although it will be desirable to combine readout electronics in this submission, integrated with the ISIS sensor, we have not made this part of the baseline plan.

2.2.3.1.7 ISIS Summary

The ISIS should be the most robust against electromagnetic interference of all of the silicon sensors currently being considered for use in the vertex detector at the ILC, a feature of great importance

given that the experience at the SLD suggests that the ILC may well be a noisy environment. The ISIS will also allow the reduction of the amount of material in the end caps of the vertex detector, as no additional drive circuitry will be required. The development of large ISIS ladders on the time-scale envisaged here represents a challenge for the LCFI Collaboration, but the rewards will be a detector that offers excellent tolerance to the problems of RF pick-up.

2.2.3.2 Flexible Active Pixel Sensors

In recent years, the UK has led development of CMOS Monolithic Active Pixel sensors (MAPS) for scientific applications^{22,23} in particular in devices with in-pixel storage. The Flexible Active Pixel Sensor (FAPS) was in fact designed specifically to cope with the beam structure of a LC based on cold RF technology. As with the ISIS sensor described above, the sensor signals are sampled during the bunch train and are stored in the pixel to be subsequently read out during the quiet, inter-train period. One difference between the sensors is that, while the ISIS stores the raw charge in a CCD register, the FAPS converts that charge to a voltage which is stored on capacitors in the pixel (which implies that this sensor is potentially more sensitive to EMI effects than is the ISIS). Column parallel readout, at only a few MHz, is then enough to capture the data from a complete ladder in a few ms, well before the arrival of the next bunch-train.

Common features of the readout electronics needed for the CPCCD, the ISIS and the FAPS will also be exploited to reduce costs, as will the synergy of the LCFI and Basic Technology MI³ programmes. The MI³ consortium is developing the underpinning technology for CMOS Monolithic Active Pixel Sensors. While this provides huge added value in terms of the establishment of CMOS sensor capability in the UK and prototyping concepts, MI³ is not mandated to provide devices for specific scientific areas of interest. Hence the need to develop the large scale FAPS needed for the ILC as part of the LCFI programme,

In the last few years, CMOS Monolithic Active Pixel Sensor (MAPS) technology has become a major competitor in solid-state imaging for consumer applications. The use of CMOS technologies for imaging devices offer great advantages in terms of integration of functionalities, pixel size, radiation resistance and ease of use. Figure 2.8 shows the main difference between a standard MAPS and the FAPS design. In this figure the schematic of a pixel in a standard MAPS is shown along with two different versions of the FAPS. In the standard MAPS, the diode is connected to a reset transistor and the input of an in-pixel amplifier. This is drawn with a dashed line because it is active only during the readout, thus minimising power consumption. When this is requested, the select transistor is activated and the voltage signal corresponding to the charge stored into the pixel is readout. Since all the pixels in a column are connected to the same output line, the capacitive load on this line is relatively large,

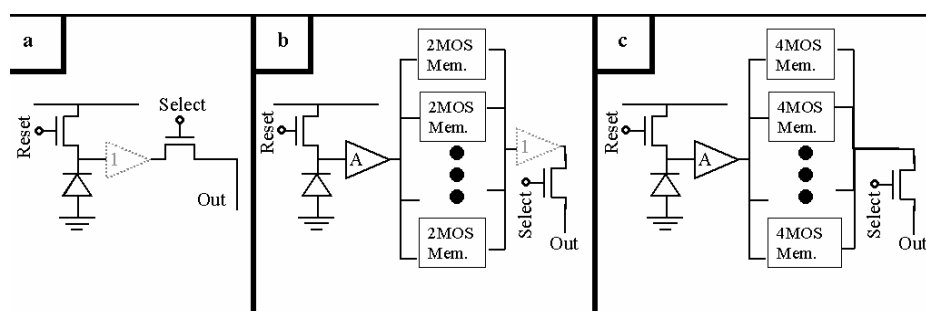


Figure 2.8 Comparison between a standard MAPS (a) and two variants of the FAPS concept (b and c).

²² N. Waltham, M. French, M. Prydderch, Q. Morrissey, R. Turchetta, A. Marshall, J. King, and G. Woodhouse, (2002), *CMOS Active Pixel Sensor Developments at the Rutherford Appleton Laboratory*, Proceedings of the Workshop on Scientific Detectors for Astronomy, June, 2002, Hawaii.

²³ R. Turchetta et al., *CMOS Monolithic Active Pixel Sensors MAPS: new 'eyes' for science*, presented at Vertex 2004, to be published in NIM A.

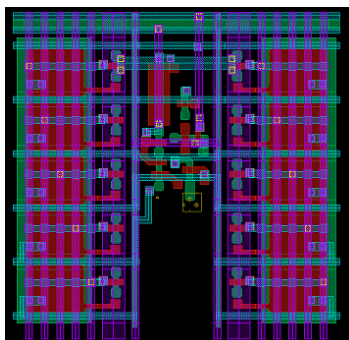


Figure 2.9 Layout of the FAPS 20 μm pixel designed in a CMOS 0.25 μm technology (HEPAPS).

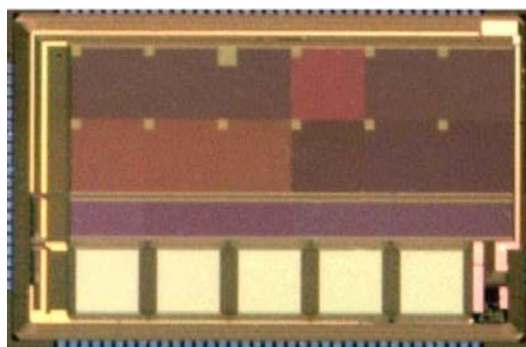


Figure 2.10 Photograph of the HEPAPS parametric test sensor, which includes variants of the FAPS pixel: five arrays of 40x40 pixels, each with 10 memory cells.

of the order of a few pF. This capacitive load limits the speed at which the sensor is going to be readout to on the order of a few 100s ns. If this number is multiplied by the number of rows in a sensor, even considering multiple readout lines, it would not be possible to readout a standard MAPS at the speed required by ILC.

To overcome this limitation, the FAPS architecture samples the signal from the photodiode inside the pixel and stores it inside the pixels until the long beam-off period in which it can be read out at a more relaxed pace. One important characteristic of the FAPS is that the combined action of the write amplifier and of the memory cell provides amplification of the charge signal. These transfers can give over an order of magnitude more signal and this can be used to improve the resistance to noise during the subsequent readout of the sensor.

Two designs are under study for the memory cells; one with only two transistors and a second one with four transistors. The storage element is a MOS transistor used as a capacitor and accessed through transistors used as switches. In both cases the readout is through an in-pixel source follower as in a standard MAPS, but while in the first FAPS design the source follower is shared between all the memory cells, in the second design there is one source follower per cell. These two designs show the flexibility of the FAPS concept and, while the second design has the advantage of keeping the cell readout independent, the first one is the favourite in terms of simplicity and compactness of the cell. It is for this reason that this design was investigated first.

2.2.3.2.1 Current Status – Results from the HEPAPS Programme

Five variants of the FAPS were constructed as part of the PPARC funded HEPAPS programme. For each variant, an array of 40 x 40 pixels was produced on a 20 μm pitch with 10 memory cells in each pixel. The layout of a 20 x 20 μm^2 pixel from this program is shown in Figure 2.9 and the final device is shown in Figure 2.10. The FAPS was tested with a pulsed light source and with a ^{106}Ru β source. Measurements were also performed in a test-beam at DESY, the analysis of which is underway. A typical example from the pulsed light source test is shown in Figure 2.11. Samples were written in the memory cells at 10 kHz and subsequently read out. A light pulse was generated during

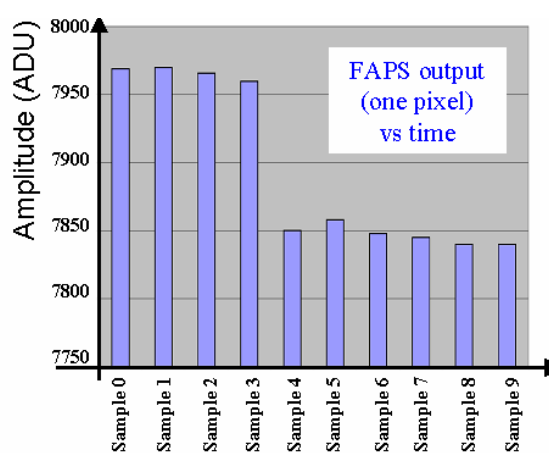


Figure 2.11 Output amplitude from the ten cells in a pixel in a test with a pulsed light source. A pulse was generated during the fifth sample. This generates a step in charge in the photodiode which is correctly reproduced by the voltage read out from the cells.

the fifth sampling, and, as expected, a step is seen in the corresponding output signal. The speed of this test was limited by the test set-up: the FAPS can be sampled at a speed of a few MHz.

The signal distributions have been measured for all ten memory cells in several arrays using a ^{106}Ru beta-source. The results from this test correspond to a minimum ionising particle signal-to-noise ratio of between 14.7 and 17.0 with an 8 μm thick epitaxial layer (shown in Figure 2.12). The beta-source signal/noise was slightly lower than that found in our other MAPS test devices and this discrepancy is under investigation. However, these results show the FAPS is a viable concept for high energy tracking applications.

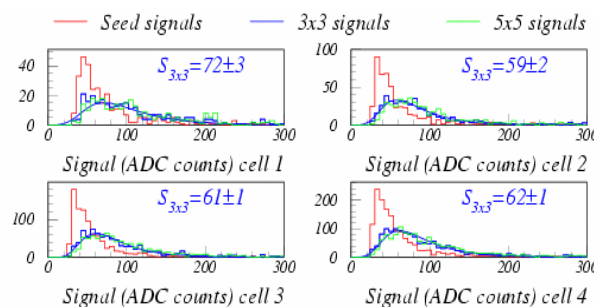


Figure 2.12 Signal distribution for the first four of the ten memory cells in one array. The S/N of cells 2 to 10 varies between (14.7 ± 0.4) and (17.0 ± 0.3) .

2.2.3.2.2 FAPS Sensor Details and Plans

The proposed FAPS development plan consists of three phases which will culminate in the production of a prototype ladder for the ILC vertex detector. Given the similarity between aspects of the ISIS and the FAPS, it may be possible to use the same foundry for both designs.

2.2.3.2.3 FAPS1 (Task 2.7: 2006 to 2007)

In the first phase, we plan to design different types of pixel architectures as in a parametric test sensor. Each section of the sensor will contain at least 64×64 identical pixels and will have a number of variants of write and read amplifiers and of storage cells. This will allow us to evaluate the pixels in terms of noise, signal, radiation hardness and readout speed. Extensive simulation of the sensor will also be done and the results compared with the experimental measurements. There is likely to be a trade-off between the size of the pixel, the readout speed and the length of time available for readout as the charge stored in a CMOS memory cell tends to slowly leak away. Mild cooling of the sensor, to around 0°C , will be explored to increase the storage time if this should prove necessary. The parametric test sensor outlined above will allow us to select the architecture which offers performance best matched to the requirements of the ILC.

2.2.3.2.4 FAPS2 (Task 2.8: 2007 to 2008)

Building on the experience gained with the FAPS1, the FAPS2 will be designed. This is likely to be a $2 \times 2 \text{ cm}^2$ uniform array. As the size of the sensor increases, the emphasis of the design effort will move from the sensor itself to the integration of the sensor in a larger system, e.g. to the design of readout circuits which will allow the integration of the sensor into a full ladder. This prototype, although still limited to the reticle size, should contain all the electronic building blocks needed for the integration of the sensor into a ladder. The readout speed will be tailored to the large area sensor. Depending on the results obtained in the first phase, this second sensor may well be a stitched device, allowing first study of any problems arising from this procedure.

2.2.3.2.5 FAPS3 (Task 2.9: 2008 to 2009)

The FAPS3 will be a ladder-scale stitched sensor. At this stage, we will consider the advantages of integrating the sensors, the analogue-to-digital circuitry and the sparsification logic on the same silicon wafer. As for the ISIS, this could result in a reduction of the amount of material in the vertex detector in the forward direction, as the need for separate readout chips would then be removed. Indeed, the electronics needed for the analogue-to-digital conversion and the sparsification logic for the FAPS will in all probability be very similar to those needed for the CPCCD and the ISIS. This is

one of the areas in which developing the three sensors within the same collaboration leads to efficient use of resources.

2.2.3.2.6 FAPS Summary

The FAPS concept, with its in-pixel storage cells, offers an interesting combination of properties for a potential ILC detector and its functionality has already been demonstrated on a small scale. It offers the advantage of using a standard stitched optical CMOS process and is likely to be able to operate at, or close to, room temperature, giving a reduction in the overall mass of the vertex detector.

2.2.4 Concluding Remarks on CPCCD and Storage Sensors

As outlined in the introduction to this section, the physics needs of the ILC, together with the unique timing and background environment of the accelerator, pose a substantial challenge to sensors design, particularly following the choice of the cold technology.

None of the sensors discussed here yet satisfies all the conditions for application at the ILC. The major remaining challenge for the CPCCD is the development of low mass drive circuitry. Concerns about achieving the necessary readout speed with a low mass drive system make it sensible to consider storage devices, such as the ISIS and FAPS. These sensors store the signals generated during the bunch train within the sensitive pixel, allowing column parallel readout at a frequency of about 1 MHz in the gap between bunch trains.

It is not yet clear which of these technologies will be able to satisfy the requirements of the ILC vertex detector on the available time scale. Fortunately, there are many synergies between the developments needed for each of these sensors, allowing the study of these options at a cost that is considerably lower than would result if they were investigated separately. The pursuit of both storage (FAPS and ISIS) and Column-Parallel CCD options within LCFI therefore gives flexibility and responsiveness to new developments, and substantially mitigates the risk associated with following a single path.

2.3 Work Package 3: Readout and Drive Electronics

2.3.1.1 Development of the CPR readout ASIC

The passage of a charged particle through the CPCCD, ISIS or FAPS produces a small electrical signal that must be amplified and digitised and then recorded for further analysis. Given the enormous number of pixels (nearly 10^9) and the low average occupancy (<1%), the digitised data must also be “sparsified”, so that only the pixels containing hit information are read out. This is done by identifying groups of pixels containing signals above the noise threshold and then performing a clustering operation so that neighbouring pixels with hit information are also recorded, even if they are below threshold. The goal of our readout development is therefore to produce electronics for the full sensor width that can amplify and digitise the signals, filter out correlated noise, impose thresholds and perform clustering and then write out the sparsified data.

These critical steps of converting the raw charge or voltage from the sensors to usable digital data are accomplished by a custom Application Specific Integrated Circuit (ASIC), the Column Parallel Readout (CPR) chip. The CPR is currently in its second generation, and is being developed by the

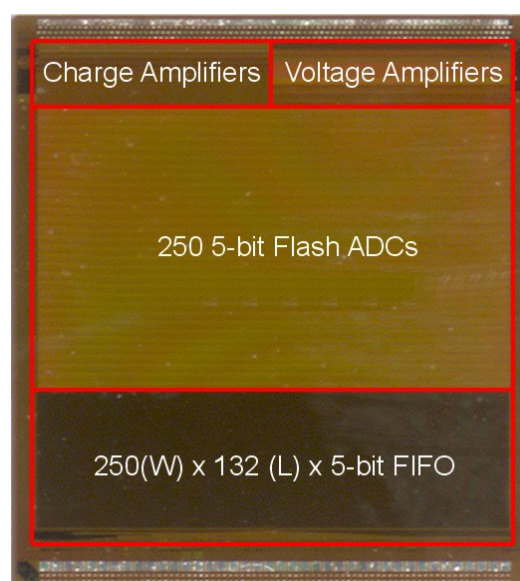


Figure 2.13 Column parallel readout ASIC (CPR1) with charge and voltage inputs.

RAL Microelectronics group, with Stephen Thomas as the CPR project leader. To date, the CPR ASICs have been produced using 0.25 μm IBM technology, through multi-project wafer submissions (MPWs) coordinated by CERN. Features of the readout chip include the ability to operate at a maximum rate of 50 MHz, compatibility with sensor outputs on a pitch of 20 microns, 5-bit digitisation, and on-chip clustering.

Development of the CPR began with the successful CPR0, which comprised three blocks of ADC layouts and direct voltage inputs. The CPR0 was rigorously tested, and results fed back into the optimisation of the design of CPR1, a scaled-up version of CPR0 suitable for wire and bump-bonding to the column-parallel CCD CPC1. The CPR1 design includes front-end amplifiers to allow use of the full ADC input range of $\sim 100\text{mV}$. Two amplifiers are implemented, one for the CCD source follower outputs, the other for direct connection to the output nodes. Shown in Figure 2.13, the CPR1 ASIC is 6 mm by 6.5 mm in size and contains 250 5-bit flash ADCs on a 20 μm pitch. It is designed to work at 50 MHz, and is currently being used for testing of the CPC1.

In the future we plan to continue the development of more advanced readout chips, for the CPC, ISIS and FAPS. Continued involvement of the RAL Microelectronics Group is essential, as the final devices are the product of careful long-term development in close collaboration with the designers and testers of the sensors. As the readout ASIC must be matched to the appropriate sensor, development of separate readout ASICs for the CPC, the ISIS and the FAPS is necessary. The readout needs of the CPC and the two storage sensors are very similar, however, as a column-parallel architecture will be used for each. It is expected that substantial sections of the design can be copied, saving on development, simulation and layout time. If the approach of using source-follower (voltage) CPCCD outputs is used, the readout chip developed for the CPC may well have a large overlap with those for the ISIS and FAPS.

2.3.1.2 Development of low-mass drive electronics for the CPC

Construction of a low mass detector module (“ladder”) using column parallel CCDs requires the development of a low-mass driver. These miniature high-current drivers must be able to provide the signals necessary to drive the CPCCD at frequencies of up to 50 MHz, with voltage swings sufficient to ensure efficient charge-transfer. Consequently, significant effort will be made to reduce the drive

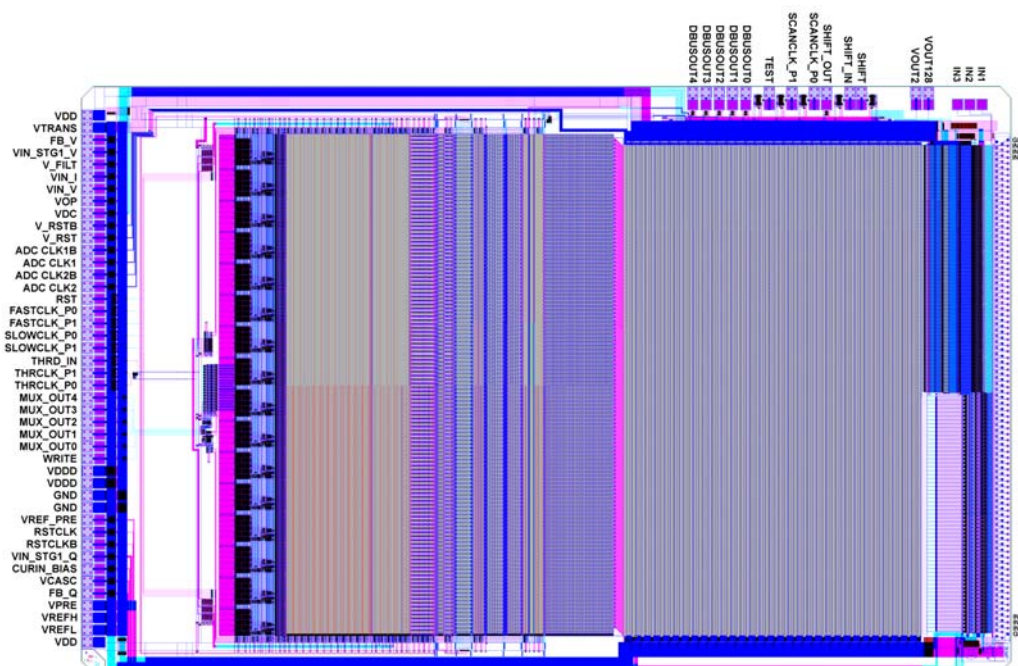


Figure 2.14 The CPR2 readout ASIC. The chip features 250 channels with (from right to left) a bump-bond field at 20 μm effective pitch, voltage and charge sensitive amplifiers, 5-bit flash ADCs, binary conversion logic, cluster finding logic, sparsification circuitry, multiplexing circuitry, and readout and diagnostic control pads.

voltage required in the CPCCD as much as possible as is described in Work Package 2. At present, the voltage necessary to drive the CPC1 is just under 2 volts.

The approach initially taken to creating a low mass driver for the CPC sensors was to provide the high current but low voltage required by means of a small transformer located very near the sensors. This approach has some limitations, however. The transformer itself is relatively large and the PCB fabrication method gives it non-negligible mass. In addition, significant current is carried by the wire bonds connecting the transformer to the CPCCD. We plan therefore to explore the possibility of a dedicated ASIC, bump-bonded at the end of the sensor, to provide the necessary clock drive. As this development work will involve the development of custom ASICs we have chosen to include it in the same work package as the readout electronics.

2.3.2 Development of readout ASICs

2.3.2.1 CPR2

The CPR2 is designed for reading out the signals from the next-generation CPCCD, the CPC2. An evolutionary development from previous readout ASICs, the CPR2 includes cluster finding logic and sparse read-out. There are also significant improvements in the performance of the amplifiers and ADCs in order to provide better uniformity and linearity. In particular, the sensitivity of the design to clock timing and power supply is much reduced. Shown in Figure 2.14, the CPR2 has been submitted for production, and should be available for detailed testing by April 2005.

The cluster finding logic works by examining successive clusters of 2 by 2 pixels. Once a 2 by 2 cluster is determined to be over threshold, an area around the cluster of ± 1 column and -2 and $+5$ rows (4×9 in total) is flagged for readout. This is illustrated in Figure 2.15. The data is then clocked out via a two-layer multiplexer circuit, which encodes information on the pixel location and the ADC signals. The CPR2 chip is driven by step voltages typically in the range 0 to -3 mV (source follower outputs) or charges of 0 to 2000 electrons (charge outputs). The voltage and charge amplifiers are designed to produce a 0 to 100 mV output step over their dynamic ranges (larger signals can also be amplified, but linearity will degrade). The charge amplifiers are split into two regions: one with 3 fF feedback (as for CPR1), the other with 2 fF. The increased gain will make the setting up of the ADCs easier. A corresponding increase in the gain of the CPR2 voltage amplifier is not required.

The amplified voltages will be sampled at up to 50 MHz with 5-bit accuracy, and the ADC outputs processed by the cluster finding logic. The number of ADC/memory channels is 250, laid out in two blocks: 125 for amplifying the CCD source follower outputs, 123 for direct connection to the CCD output nodes. In addition, one voltage amplifier samples the CCD reset voltage, and one ADC channel directly measures its pre-charge voltage. These two channels will be useful for evaluating ADC noise, crosstalk and CCD clock feed-through. A digital test register is also provided which serves a number of functions: serial output of the ADC bits for all channels before cluster finding; input of data to the cluster logic for test purposes; selection of 5 ADC bits from a single channel for high-speed parallel output.

In addition to the new features of the CPR2, the deficiencies observed in the CPR1 have also been corrected. The primary difficulty in operating the CPR1 was traced to clock skew and delay issues. These were addressed by regenerating the clock locally in each comparator cell of the ADC (using an inverter). The difficulty arose in the block responsible for switching between V_{in} and V_{ref} in the ADC, and it illustrates the challenges faced in making a large and complicated ASIC. Although simulations showed that the timing of this switching was good for 10 cells, the full 250 cell width could not be simulated. Once fabricated, the timing over the full width was seen to be off by as much as 10 ns. The result was a chip that showed gain variations over the voltage amplifier channels, with approximately 10% of these channels not functioning. This lesson clearly illustrates the need for progressing carefully to a full width device.

2.3.2.2 CPR2a

A number of changes are needed to make the CPR devices a viable readout chip for final ladders in a test-beam. The chip must be simpler to operate, faster, and able to read out the full width of a CPCCD sensor. As the CPR is a mixed mode (analogue and digital) ASIC, some of these changes affect the digital part of the chip and some the analogue. For example, we need to make a wider readout chip, and one with on-board voltage generation to greatly simplify the control and operation of the device. We expect that the onboard generation of voltages will require careful attention to the analogue part of the ASIC, but should have no effect on the digital. Similarly, making a much wider readout ASIC (much more than the 250 channels of CPR2) could have an impact on the digital design, but not the analogue.

In progressing towards a readout ASIC sufficient for full-scale ladders, we plan to separate these improvements into several development cycles. We will first address the problems posed by the complicated interface to the readout ASIC. One way to make the CPR2a easier to use is to reduce number of voltages that must be supplied, thereby reducing the number of connections required. This will be accomplished by on-chip analogue bias generation, with programmable levels (controlled by serial registers). This will eliminate many of the analogue control pads, and will make adjustments easier.

We will, of course, also address any deficiencies we find in CPR2. Indeed we will have much to learn from the bump-bonded CPC2 and CPR2. One concern is the possible increase in digital noise in the CPR2 (for example from regeneration of the clocks in each comparator of the ADC). If this is the case, we may consider moving to on-chip waveform generation and the derivation of all the internal clocks from a single external master clock. This further reduces the number of pads and simplifies the interface, allowing fine tuning by programming internal delays under software control rather than by using complex external drive electronics. If, however, we see little increase in noise, we can re-use these blocks, and we may well keep for the moment the complicated clock sequencing interface.

The CPR2a will be designed to be compatible with the CPC2 and will be the same width as the CPR2, hence the designation “2a”.

2.3.2.3 CPR3

With the CPR3 we will begin to address the significant challenges of making a wide readout chip. We expect to only use one type of readout amplifier at this point. The CPR3 will be designed to be fully compatible with the widened bump-bond field of the CPC3 sensors, which will have about 500 channels. The goal of this submission is to at least double the width of the CPR2a, while maintaining full functionality and allowing bump bonding to the CPC3. It should be noted that this change is sufficiently ambitious that, if we choose not to include on-chip waveform generation on the CPR2a, we will most probably not introduce it here.

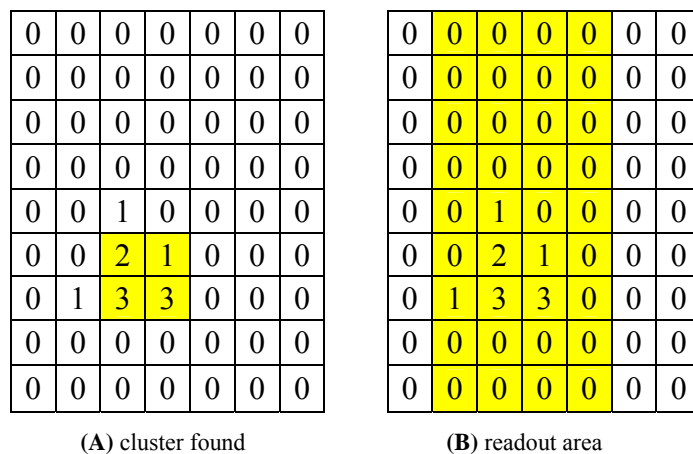


Figure 2.15 Sparse readout, based on cluster finding. In the example above, a 2 by 2 cluster threshold of 8 is applied. Although each pixel is below threshold, the 2 by 2 sum (A) is above threshold, causing a block of 4 by 9 pixels to be flagged for readout (B).

2.3.2.4 CPR4

The CPR4 will be a fully functional CPR chip for bump bonding to the CPC4. This is

the final readout chip, meant for placement on ladders for the final beam tests. The development and final placement of the CPR4 will be coordinated with both the CPD4 and the CPC4, as it will have to be placed on a thinned sensor with the final drive electronics attached.

2.3.2.5 CPR-ISIS3

The CPR-ISIS3 is a dedicated ASIC drawing much of its design from the CPR2 and CPR2a. It will feature column parallel readout but it is not likely to be possible to use directly the CPCCD CPR ASICs for the ISIS readout because of the different time structure of the outputs. This chip will be made to be bump-bond compatible with the ISIS3 sensors.

If the ISIS sensors can be made on 0.25 μm or smaller technology (e.g. at Jazz Semiconductor), we are considering also including a readout chip in the same wafer submission as the ISIS sensors. We may choose to include this as a stand-alone ASIC or to connect it directly to the ISIS sensors, hence avoiding the problems of bump bonding the readout ASIC to the sensor. This will of course require careful investigation, but as we are likely to have full control of an engineering run (owing to the large scale stitched devices being produced) we can include several options in the submission. A monolithic ISIS sensor plus readout on the same thinned silicon, without the need for bump bonding, is an extremely attractive option.

2.3.2.6 CPR-ISIS4

The CPR-ISIS4 readout will be the readout ASIC for ISIS4. This may be bump-bonded to the sensor, or, if the more ambitious monolithic solution proves possible, the readout and the sensor may be integrated on one silicon wafer.

2.3.2.7 CPR-FAPS2

The similarities between the two storage sensors, the ISIS and the FAPS, mean that much of the development of the FAPS readout will be common to that of the ISIS. Exceptions include the amplification stage where, due to the amplification provided on the FAPS, smaller gain will be needed on the readout chip. Further, the algorithms needed to filter out correlated noise will differ somewhat, as may details of the cluster finding, where sensor dependent tuning may be necessary.

2.3.2.8 CPR-FAPS3

The CPR-FAPS3 is the final readout ASIC, for the FAPS3 sensor, It will incorporate the results of the CPR-FAPS2 development, and like CPR-FAPS2 this ASIC will differ with the CPR-ISIS4 due to differences in sensor properties and front-end architecture. The CPR-FAPS3 will be made to be bump-bonded to the FAPS3 sensors, although integration of readout and FAPS3 on one silicon wafer may be possible.

2.3.3 Development of driver ASICs

2.3.3.1 CPD2

The CPD2 will be the first ASIC-style solution to the challenge of developing a low-mass driver for the CPC sensors. We are currently considering two options, either a power CMOS buffer (producing essentially a square wave of the requisite voltage) or a power CMOS OpAmp (which allows an arbitrary waveform). This device will be wire-bondable only, and will be compatible with the CPC2.

2.3.3.2 CPD3

The next development for the CPC drivers (CPD3) will be an ASIC designed to be bump-bondable to the CPC3 and should provide a suitable driver for the innermost layer of the vertex detector. In this layer the overall size of the ladders is smaller, so the overall current is lower. As illustrated in Figure 2.16, the driver ASIC will be bump bonded between the sensor and the readout. Inverting the

positions of these chips leads to unacceptable losses when transporting the drive signals past the readout chip.

2.3.3.3 CPD4

The final ASIC submission will concentrate on making a bump-bondable driver, the CPD4, which is compatible with the final CPC4 sensors. The challenge will be to make a driver that will work for the outer layers of the vertex detector, where the required current is perhaps twice that of the innermost layer.

The drive chip will require significant power, the provision of which requires cables that would add an undesirable amount of material to the vertex detector. This can be avoided by using a high value capacitor, of the order of 0.3 F, which is charged up during the inter-train period and from which the chip draws its power during the bunch train.

2.4 Work Package 4: External Electronics

In addition to the sensors themselves (described in work package 2), the readout chips needed for each of the sensor types and the drive chips needed for the CPCCD (described in work package 3), a considerable range of electronic systems are needed for the proposed LCFI programme. Printed circuit boards must be designed for the testing of the various CPCCD, ISIS and FAPS generations, in both standalone mode and in conjunction with the readout and, where appropriate, drive chips. Further boards are also needed for testing of the readout chips themselves. Data acquisition and control systems must be provided to steer these chips and capture the data they produce. Boards for the testing of the CPCCD drive systems must also be designed.

As the design of the drive circuitry for the CPCCD is challenging, and it is not clear that a system based on an Application Specific Integrated Circuit (ASIC) will provide the necessary performance, an alternative transformer-based drive solution is under investigation. This will be used for tests of the earlier generations of the CPCCD and may be the device of choice for the full scale modules (“ladders”) to be produced at the end of the current programme.

The beam tests of full scale CPCCD, ISIS and FAPS ladders will require the development of further electronics. These are the systems that will steer the operation and readout of the vertex detector sensors in the ILC detector.

The design and development of all these systems is the subject of this work package.

2.4.1 CPCCD electronics

2.4.1.1 Transformer based drive circuit

One approach to the drive of the CPCCD, described in the WP3, is

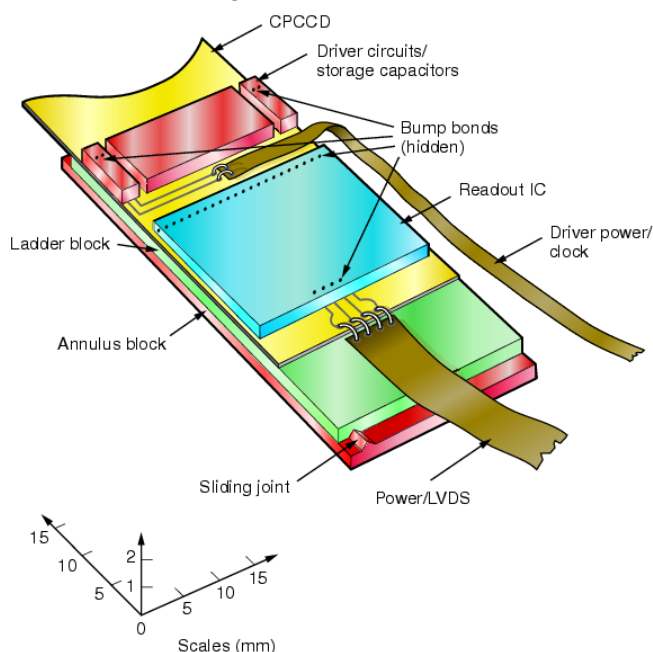


Figure 2.16 An illustration of the end of a CPCCD ladder showing the drive ASIC bump-bonded between the readout chip and the sensor and the capacitors used to store the power needed for the drive.

the development of an ASIC which can be bump-bonded to the CPCCD. This device will draw significant power while the CCD is being read out and transmitting this directly to the ASIC would require large diameter cables. At the ILC, these would represent not only undesirable material, but also an additional load on the cryogenic system due to the heat they would conduct into the cryostat. Alternatively, as is discussed in the previous section of this report, the necessary power can be stored locally in a capacitor of value around 0.3 F which can be charged up through a small cable during the long inter-train period. However, there are questions regarding the number of charge cycles such capacitors will tolerate, their radiation hardness and the effects of low temperature operation. Problems arising due to the last of these points could be ameliorated by placing the capacitors outside the cryostat at the ILC, but only at the expense of again introducing large diameter cables to carry the necessary current into the cryostat.

In case the above problems prove insurmountable, and to provide an interim system for tests of the CPC2, a second drive solution is under investigation. This uses transformers placed at the edges of the CPCCD to provide the low voltage high current 50 MHz signal needed to ensure adequate clock voltages across the imaging area, with its relatively large capacitance. The input to the transformers can then be a high voltage RF signal, allowing the necessary power to be delivered to the system through relatively small cables. Initial designs of this drive foresee the use of an air-core 16-to-1 device of 1 cm diameter fabricated on an eight or ten layer PC board and simulations indicate that such a transformer, wire bonded to opposite corners of only one end of a sensor (i.e. the CPC2-40), should give acceptable performance up to 50 MHz. First transformer designs have been produced and tested, some of which are shown in Figure 2.17. Currently, the transformer itself is relatively large and the PCB fabrication method gives it non-negligible mass. Future developments of this drive option will include the reduction of the mass of the transformer system as far as is possible and the study of the behaviour of the multiple wire bonds which transmit the drive signals from the transformer to the CPCCD.

The transformer based system now available will be used for standalone tests of the CPC2 and for tests of the CPC2 bump bonded to the CPR2 and CPR2a. This will be adequate for the small CPC2-10 chips if attached only at the lower corners of the CCD and is likely to suffice for the CPC2-40. It is not clear, however, that it will be able to provide clock signals across the full area of the larger CPC2-70 if the signals are input only at the lower corners of the CCD. Both the CPC2-40 and the CPC2-70 are therefore provided with clock monitoring and drive pads at every 6.5 mm along their length, allowing the input of clock signals at many points along the CCD if required. The transformer-based drive will thus be adequate to demonstrate the functionality of these CPCCDs.

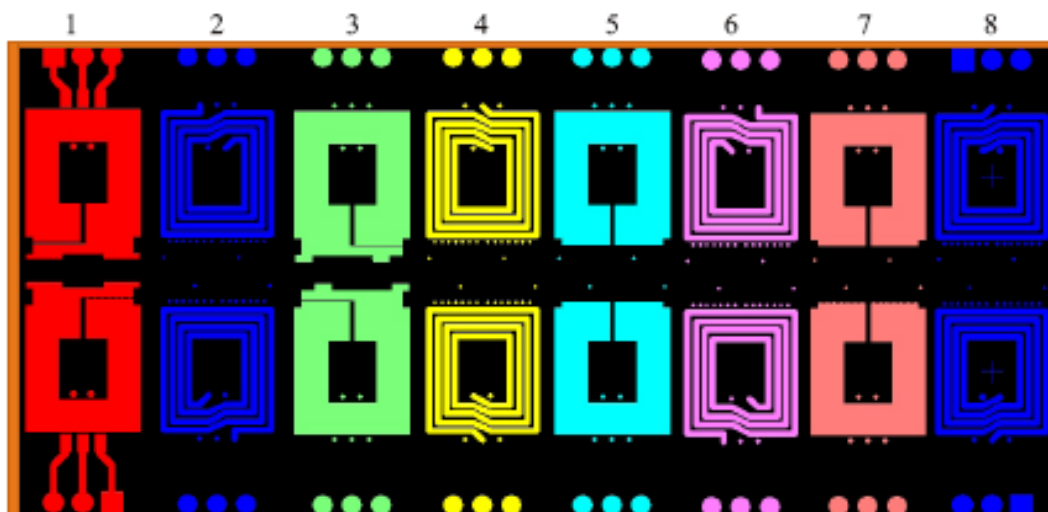


Figure 2.17 An eight layer printed circuit board for the testing of a range of CPCCD drive transformer designs.

Development of both the ASIC and transformer based drive systems will be facilitated by the use of Spice models which will be tuned using the data obtained from measurements of the CPC2 and the “passenger” CCDs produced following the CPC2. These will serve as an aid to the understanding of the requirements on the drive systems and, in particular in the case of the transformer based option, allow the investigation of novel ideas such as exploiting resonance in the CPCCD drive circuit to minimise the power consumed.

The design of the later drive systems will depend on the progress made with the CPD, which in turn is dependent on the results of the tests of the “passenger” CCDs. As described in Work Package 2, one of the goals of this series of test devices is to explore how the load the CPCCD represents to the drive system can be reduced. If these developments make ASIC based drive systems more attractive than the transformer based option, the latter will not be further pursued, though they may be employed for standalone tests of the later generations of CPCCDs, as described below. If it proves unlikely to drive the CPCCD using an ASIC, studies of the transformer option will continue.

2.4.1.2 Printed circuit boards for CPCCD, CPR and CPD tests

A further challenging project is the development of the many boards needed to test the CPC3 and the CPC4. These must deliver the required 50 MHz high current drive to the CPCCD and accept small signals with large bandwidth from it without introducing noise. Further, they must provide all necessary bias voltages for the CPCCD. Each generation of CPCCDs will require two sets of boards on which they can be tested. The “standalone” boards will allow testing of the CPCCDs without bump-bonded readout and drive chips, while the “motherboards” will allow testing of the CPC and CPR assembly, with either the CPD or transformer based drive systems. In addition to the bias voltages for the CPCCD, the motherboards must provide the bias and clock voltages needed for the CPR. These systems will be designed around a 0.8 mm deep well in the printed circuit board that can hold either a CPC in the case of the standalone boards or, in the case of the motherboards, a multi-chip module consisting of a CPC onto which a CPR and possibly a CPD have been bump-bonded.

The standalone boards will feature clock drive electronics which can be wire-bonded to the CPCCD using either the transformer based system described above or a driver chip. For test purposes, the latter may be a commercial system or a CPD. The boards will be equipped with low noise amplifiers which will amplify the analogue signals coming from the CPCCD prior to their digitisation and processing. These boards will need temperature monitoring and protection circuits to prevent overload of the CPCCD clock networks.

Boards similar to those needed for the CPC3 and CPC4 will have to be constructed for the “passenger” CCDs.

A further set of boards must be developed for standalone tests of the CPR chips. Three readout test boards will be constructed, allowing the testing of the CPR2A, CPR3 and CPR4 systems. They will be equipped with a subset of the electronics found on the CPC motherboards which will provide the CPR with clock and bias voltages and allow the readout of the digital signals produced by the chips. In addition, these boards will feature circuits that can inject analogue signals into the readout chip’s input.

In order to allow standalone testing of the transformer-based drive, CPD2, CPD3 and CPD4, individual test boards will be constructed. These will provide loads that are equivalent to full CPCCD inner and outer layer detector modules, allowing investigation of the electrical performance of the drive systems.

2.4.2 Storage Sensor Electronics

2.4.2.1 Test boards

A similar series of boards to that required for the development of the CPCCD and its readout will be needed for the ISIS and the FAPS. The test board for the ISIS1, which requires external drive, has already been designed and this sensor will be tested as soon as it is delivered on this board.

Test boards for later generations of the ISIS and the FAPS are likely to be closely related to each other, as both the signals needed to control these two sensor types and the signals they produce are similar. Neither the ISIS nor the FAPS designs presented here require external drive circuitry as this functionality is provided on chip. It is proposed that the test boards for the ISIS2 and later generations of the ISIS and for the FAPS will be designed by the RAL Instrumentation Department and assembled in industry.

2.4.3 Data acquisition and control system

The data acquisition and control system that the LCFI Collaboration has used so far is based around a VME mother board to which various daughter boards can be attached. These provide control of the amplitudes and phases of the CPCCD drive and sequencer signals which steer the data acquisition and involve control of delays at the sub-nanosecond level. The system also controls the supply of the bias voltages for the CPCCD and the voltages needed for the CPR chips. If standalone tests of the CPCCD are being performed, the system controls the amplification, filtering and digitisation of the analogue signals from the CCD output nodes. If the readout is being done via the CPR chips, the system captures the digital data these produce.

Programming of the VME system is done using LabVIEW and significant effort is also invested in developing the firmware for the Field Programmable Gate Arrays (FPGAs) that are used to generate the fast signals necessary to steer the CCD drive and readout.

Current plans foresee that tests of the CPCCD will continue with VME based systems. However, the RAL Instrumentation Department now has considerable experience with systems based on FPGAs with embedded gigabit Ethernet. Indeed, the group currently working on Monolithic Active Pixel Sensors which developed the FAPS concept performs its testing using such a set-up. The hardware necessary for this option is cheap and the resulting systems are very powerful. With the help of these new collaborators, the LCFI collaboration will use this concept for the testing of the ISIS and the FAPS and will move to using such a system for the CPCCD when it is opportune to do so. As is discussed further below, the “off-detector” electronics used for full ladder tests will make use of this concept.

2.4.4 Additional electronics for beam tests

2.4.4.1 Remote Electronics

In order to satisfy the requirements of the vertex detector technology comparison, full scale ladders must be tested with electronic systems that would be suitable for application at the ILC. For example, the drive and readout of the CPCCD ladder must be incorporated at the end of the ladder, and the necessary control signals generated in “remote” electronics. Similar considerations apply for the ISIS and FAPS, where the readout may be incorporated on the same wafer as the sensor, but control signals will be provided by external electronics. At the ILC, these remote electronics will be located close to the beampipe outside the vertex detector, with the connections between the two systems running along the beam pipe.

An important consideration in the design of the ladders and the remote electronics is that the material budget be minimised. This implies that the number of connections between the end of the ladder and the off-ladder systems must be reduced to the minimum compatible with providing the necessary power and control signals and extracting the data. The number of power cables fed in to the vertex detector must be reduced as far as possible, for example by generating as many as possible of voltages necessary to bias the sensors and power the readout electronics at the end of the ladder. The sparsified data produced by the sensor readout will represent the majority of the data that must be transferred from the ladder to the data acquisition system. However, small amounts of data may also be produced by devices which record the temperature of the ladder and perhaps other environmental parameters such as the humidity inside the cryostat. It may also prove necessary to incorporate an alignment system on the ladders, the data from which must be recorded. All these systems require power and external control. The technologies to be used for the transmission of this data and control information must be defined, the necessary interfaces designed and the required software developed.

The tasks described here can only be defined rather generically at the moment. More detail will require information on the facilities at the proposed test-beam site that are not yet available. For example, in collaboration with many of our European colleagues, LCFI is bidding for Framework 6 funding for the test-beam infrastructure needed for a vertex detector technology comparison (to be constructed at DESY). This would provide some basic elements of test-beam, beam telescope, and beam telescope data acquisition system; the LCFI readout would then have to be designed to interface with this.

2.4.4.2 Summary

The production of the external electronics required for the operation of the CPCCD, the ISIS and the FAPS will require significant engineering effort. The tasks involved are not simple. This applies particularly to the drive system for the CPCCD, but production of the multitude of systems necessary to test the CPCCD and its drive, the ISIS the FAPS and the readout for these sensors will also require sustained expert engineering involvement in the project. Once functioning sensors have been produced, further design work will be necessary to produce systems that are satisfactory prototypes for the ILC vertex detector.

2.5 Work Package 5: Integration and Testing

The integration and testing work package provides the main link between sensor design, integrated readout and external electronics. Its success depends to a great extent on the completion of the tasks in WP2, WP3 and WP4. The test programme is challenging and time consuming but provides the all important results on device and system performance, vital to the LCFI programme.

The work with CPC1 and CPR1 has been the key in gaining more experience with these advanced semiconductor devices and the process of bump bonding. Both chips have performed very well and

the concept of a CPCCD bump-bonded to a readout CMOS ASIC was proved on the first attempt. The clock frequency achieved for CPC1 was much higher than the 1 MHz originally envisaged. One version of the device was shown to function with clock amplitudes as low as 1.9 V peak-to-peak. CPR1 showed full functionality of its ADCs, signal amplifiers and digital logic. Using these results, the CPC2 and CPR2 were designed and are now in advanced manufacturing stage.

Many important lessons were learned in the testing of CPC1 and CPR1 and we are confident that the programme for the next generation of devices will proceed successfully. Foreseen are studies of gradually increasing complexity, starting from stand-alone chips and progressing towards fully bump-bonded assemblies. This implies a substantial work load because of the studies of the new sensors and the new CPCCD driver chips, and it poses new challenges in term of efficiency and organisation of the work. Much tighter coupling between WP4 and WP5 will be necessary to reduce to the minimum the lead time associated with the manufacture of test boards. In the closing stages of the programme, WP5 will culminate with the delivery of tested devices suitable for mounting on prototype ladders and tested in a beam.

2.5.1 Current status

2.5.1.1 CPC1 and CPR1 tests

The tests of the first CPC1 in stand-alone mode began in May 2003, immediately after its delivery. This device, which has metallised gates, was operated successfully at 1 MHz with a RMS noise level of $55 e^-$. The minimum clock amplitude necessary to achieve efficient charge-transfer in the device with the lowest inter-gate barrier implant was 1.9 V peak-to-peak, which is a significant achievement. Minimizing the clock amplitude is a very important means of reducing the requirements on the clock drivers and the overall power dissipation. Furthermore, X-ray signals were observed at clock rates of up to 25 MHz, this frequency being limited by the available clock drivers and the asymmetry in the on-chip clock distribution due to the single level metallization.

The CPR1 chip was simultaneously tested in the RAL Instrumentation Division (ID) and in the CCD lab at RAL PPD. In the ID tests, the chip was placed in a commercial IC test station which offers great flexibility in testing timing and amplitude levels and was invaluable in investigating the intricate details of its operation. In the PPD tests, the chip was tested with the discrete electronics that were later incorporated into the CPCCD motherboard. These tests were important in the design and debugging of the electronics using realistic signals, and complement each other and are crucial to understanding the complex behaviour of the readout chip.

After the successful stand-alone tests of CPC1 and CPR1, several CCD outputs were wire-bonded to the corresponding voltage or charge inputs of CPR1 and the first X-ray signals detected in CPC1 and amplified and digitised in CPR1 were observed. The voltage amplifiers produced good quality signals and their performance was largely unaffected by the parasitic wire bond capacitance. In contrast, the charge amplifiers showed large common mode noise which was expected because of input load from the wire bond capacitance. These tests proved the principle of operation of a CCD connected to a CMOS chip and were an important milestone. Although a major success, tests of the wire-bonded assembly only allowed the study of a limited number of channels. The full characterisation of the hybrid assembly was subsequently carried out using the bump-bonded configuration.

Bump bonding is an essential step to achieve optimal performance since wire-bonding introduces parasitic capacitance to the CCD outputs. The CPC1 and CPR1 were successfully bump-bonded at VTT (Finland) using eutectic solder connections on 20 μm effective pitch. In total, 13 assemblies were delivered to LCFI in two batches. Figure 2.18 (left) shows one assembly in a test board. Initial tests revealed that, although some readout chips did not work, several assemblies performed very well. Figure

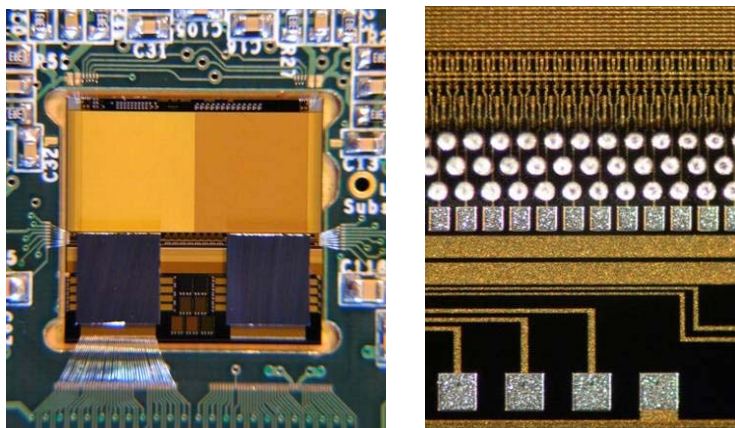


Figure 2.18 CPC1 bump-bonded to two CPR1 chips in a motherboard (left); bump bonds on a CPC1 after removing a failed CPR1 chip (right).

2.19 shows the X-ray spectra from a ^{55}Fe source (which produces primarily 5.9 keV photons, generating 1620 e^- in the CCD) from the voltage and charge channels. The noise in the voltage section is 60 e^- RMS and in the charge section is around 100 e^- RMS. Every third charge channel exhibited much larger noise due to the parasitic capacitance of the larger wire-bondable pad attached to these outputs (these pads have been removed in the CPC2 design).

All ADCs and charge channels worked well, but about 20% of the voltage channels consistently did not show any signal in all chips, at random locations. The cause of this is still unknown. A gain drop of 50% towards the centre of the voltage amplifier array, as seen in Figure 2.19 (left), was also observed. This is probably caused by clock skew and has been addressed in the CPR2.

Initial bonding yields were disappointing (30%). Defects studied are consistent with mechanical damage during pre-bonding compression misalignment. After consultation with the vendor we have taken several steps in the design of CPR2 and CPC2 to reduce the risks in the next bump-bonding cycle. There are now 3 edge bump bonds for the CPR2 instead of one, and the thick aluminium tracks on the right hand side of the CCD have been removed. Furthermore, the readout chips will not be thinned before bonding which will help reduce the mechanical stresses. The procedure for pre-bonding alignment and chip attachment will be refined, and the compression force of the softened bumps better tuned.

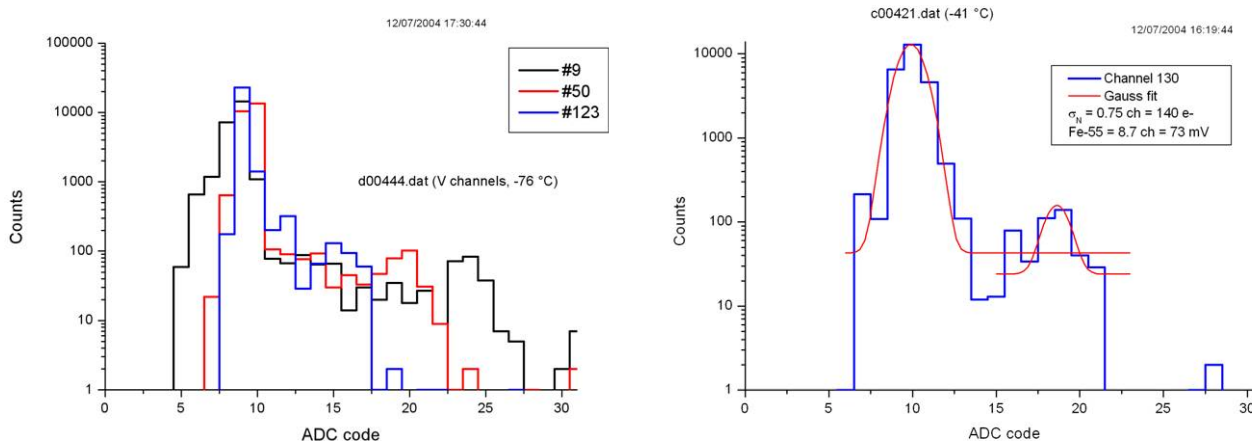


Figure 2.19 X-ray spectra in the voltage section (left) and charge section (right) of the CPC1. The gain is observed to decrease towards the centre of the voltage amplifier array, channel 123, when compared with that at its edge, channel 9.

Bump-bonding is an important part of the manufacture of good quality CPCCD, ISIS and FAPS hybrid assemblies and achieving high reliability is essential. Many HEP experiments have used this process, and VTT, to bump-bond their chips to a sensor, and all are thinned devices. The number of bonds and the complexity of these assemblies are far greater than required for LCFI, and we hope that the problems we have seen so far can be ironed out for the bump bonding of CPC2 and beyond.

2.5.2 Future tests of CPCCD and Storage Sensors

2.5.2.1 Evaluation of the CPC2-based hybrid assemblies

The CPC2 will be manufactured and delivered by July 2005. There will be 3 different sizes of chip (13 mm, 52 mm and 91 mm long) devices with standard single level metal and busline-free 2-level metallization. All will be tested stand-alone in the CCD Lab. in the RAL PPD using a motherboard with on-board amplifiers for the groups of 4 adjacent source followers. This will give us insight into several important CCD parameters: sensitivity, maximum operating frequency, noise, minimum clock amplitude and effective gate capacitance. The CPC2 will be clocked using miniature transformers connected to a commercial power RF amplifier, as described in Work Package 4.

At the same time, CPR2 will be tested in parallel in the CCD Lab. using a test board. This will enable us to understand the behaviour of the chip and help design the electronics for the second version of the motherboard, which will allow testing of bump-bonded assemblies of CPC2 with CPR1 and CPR2. The operation of the cluster finding logic and sparsification will be verified by supplying simulated patterns of hits to the chip test register. This will be an important step towards successful operation of the bump-bonded assembly.

CPC2 chips will be sent to VTT to be bump bonded to CPR1 and CPR2 immediately after the first single level metal devices become available. By the time the assemblies are shipped back to RAL, the behaviour of CPR2 should have been well characterised. The hybrid assemblies CPC2/CPR1 and CPC2/CPR2 will offer a wealth of information about the performance of the analogue amplifiers in CPC2, the cluster finding logic and the sparsification with real signals. The numerous test features incorporated in CPR2 will provide greater insight into the operation of the chip. Monitoring pads at the outputs of voltage and charge amplifiers will enable us to see the analogue signal waveform, which was not possible in CPR1. The digital output from any ADC channel will also be available for detailed observations.

The next CPC2-based hybrid will use CPR2a instead of CPR2 and will be clocked by the first generation driver chip CPD2. As before, CPR2a will be tested extensively both in the RAL ID and in the CCD Lab. using a dedicated board. The results from the tests will help select the output architecture for CPC3 and CPC4, which will have deep implications to the design of the next generation readout chips as well.

2.5.2.2 Experimental CCD test structures

A range of improvements to the parameters of CPCCDs will be pursued before the production of CPC3, as is outlined in Work Package 2. This will allow quick and inexpensive investigations into the possibility of low clock drive and reduced inter-gate and parasitic capacitance. Relatively simple structures will be required to study the capacitance and the measurements can be carried out with a precision LCR meter on a probe station. The studies of the clock amplitudes need simple CCD structures, which can be mounted on test boards, placed in a cryogenic environment and illuminated with X-rays from a ^{55}Fe source. The investigations would consist of measurements of the charge-transfer inefficiency (CTI) as a function of the clock amplitude. The onset of high CTI is seen at the point at which the clock amplitude becomes insufficient to overcome the inter-gate potential barrier.

2.5.2.3 Evaluation of the CPC3- and CPC4-based hybrid assemblies

The assemblies based on CPC3 and CPC4 will be very close to the final goal of building prototype ladders. Both will have fully bump-bonded readout and driver chips. In the same way CPR3 and CPR4 will be tested extensively on custom PCBs at the same time when the chips are being bump-bonded elsewhere. Some CCDs will be thinned to approximately 50 μm and could be used for charge collection studies with IR pulsed laser, shining from the back. The hybrid assemblies will be subjected to detailed tests, and in the case of CPC4 the work will be carried out in conjunction with WP6 and WP7 to enable mounting on prototype ladders.

2.5.2.4 Evaluation of the ISIS

The pilot ISIS1 device designed by e2v will be manufactured in the same wafer batch as the CPC2. The purpose of this device is to prove the operating principles of in-situ storage image sensors and provide us with first experience of these new sensors. The chip will be tested with X-rays from a ^{55}Fe source and pulsed visible light. The punchthrough voltage is the most important parameter; this will be measured with a visible light stimulus. Additional measurements will include the full well capacity, noise levels, the range of operating voltages, crosstalk and parasitic charge collection in the CCD storage register.

The numerous ISIS2 devices manufactured using a CMOS process will be tested extensively in order to evaluate their performance and potential. Both single cell and array ISIS structures will be designed and evaluated. Each device will be mounted in a test board and tested in the standard way using ^{55}Fe X-rays in a cryogenic environment. Because of the multi-level metallization, tests with visible light could be difficult. However, back-illumination using a focused IR laser could be an alternative. The main parameters of ISIS2 which must be measured are the channel potential, CTI, charge collection time, full well capacity, noise, the range of operating voltages, crosstalk and the level of parasitic charge collection into the CCD register. Additionally for the circular ISIS2 the measurement of the charge-transfer time between the photogate and the storage gates will be mandatory.

The ISIS3 and ISIS4 will be evaluated in a similar manner to the CPC3 and CPC4. These devices do not require dedicated driver chips, which will make them easier to use. Bump-bonding to the CPR-ISIS3 and CPR-ISIS4 could still be necessary if it proves impossible to produce the readout ASICs using the ISIS CMOS process. Both sensors will be thinned to approximately 50 μm for studies of charge collection times with an IR pulsed laser.

2.5.2.5 Evaluation of the FAPS

The first LCFI studies of Flexible Active Pixel Sensors will start with the testing of the FAPS1 range of small devices. These will have various different write and read amplifiers and different types of storage cells. The parameters that will be measured include noise levels, readout speed, radiation hardness and the behaviour of the storage cell. The effects on the latter of operation at reduced temperature will be investigated. Tests will be performed with a pulsed light source and with a ^{106}Ru β source. For these tests, the FAPS will be mounted on a test board, but this can be relatively simple since the FAPS does not require external drive circuitry. These tests will help to define the pixel design for subsequent FAPS generations and also the modifications necessary to the CPR chips to match them to the these sensors.

The FAPS2 will be evaluated in standalone mode and then with the CPR-FAPS readout. These tests will allow problems with increasing the size of the FAPS to be ironed out before production of the full scale FAPS3. Testing of the FAPS3 may involve the production of a bump-bonded FAPS/CPR-FAPS assembly, but this may be unnecessary if the readout chip and sensor can be produced on one wafer.

2.5.2.6 Radiation damage studies

The CPCCD and ISIS devices have to undergo detailed radiation damage studies. First indications are that FAPS technology will tolerate large radiation doses, but this will need to be characterised as a

new CMOS process may be used. In the case of the CPCCD, the main concern is the bulk damage caused by e^+e^- pairs and neutrons. Due to the large number of charge-transfers (2500 for layer 1, 6250 for layers 2 to 5 of the vertex detector) the devices are extremely sensitive to very small concentrations of radiation-induced defects. Signal electrons are trapped by the defects and then released at a later time, resulting in charge-transfer inefficiency which shows itself as loss of signal charge. Furthermore, the charge losses depend strongly on the operation conditions – temperature, signal size, clock timing and the presence of background charges (“fat zero”) are all significant. These effects can be studied in detail using the CPC2 and its source follower outputs. The throughput of the measurements could be increased considerably if the performance of the CPR chips is satisfactory and they can be used for charge detection. The statistics would then be greatly improved because 250 CPCCD columns could be used instead of just the 4.

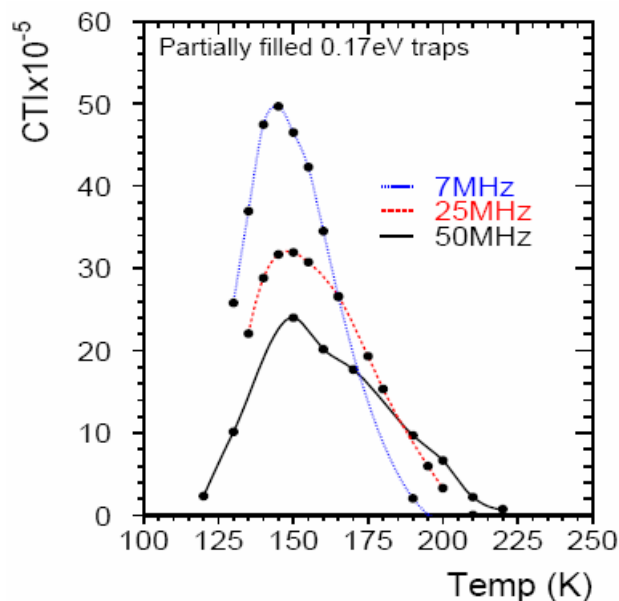


Figure 2.20 Simulated CTI in the 3-phase CCD58 for the V-O centre at $E_c=0.17$ eV.

Surface radiation damage is expected less of a problems for the CPCCD because the expected dose of 20 krad/year is well within the limits of CCD technology. However, operation at very small clock amplitudes could be disturbed by unforeseen differences in charge build-up in the 4 different levels of polysilicon that constitute the image gates. Another potential weak spot is the stepped nitride barrier because of the non-uniform dielectric thickness. The trapped charge could accumulate at different rates in the different thicknesses and this could cause drift of the inter-phase potential barrier during the lifetime of the devices. A simple and widely used method of studying the surface damage effects is to irradiate the devices with ^{90}Sr β -source.

In contrast with the CPCCD, the CTI caused by bulk radiation damage in the ISIS chips is expected to be insignificant because only 20 charge-transfers are necessary for the linear ISIS (and even fewer for the circular ISIS). However, the study of possible surface damage effects is mandatory because of the very small voltages involved and because the polysilicon gates in the CCD storage cells will not overlap but have small gaps. The rates of charge trapping under the gates and in the gaps are different and this could cause potential pockets or bumps, which disturb the smooth charge-transfer. In CCDs this can easily be corrected by changing the clock potentials, but in the CMOS-based ISIS devices, the flexibility to do this is restricted severely due to the low voltages available on chip. Most of the radiation damage studies will be carried out on the many different flavours of ISIS2 devices. The results should be sufficient to allow us to select the most radiation hard structure for the ISIS3 and the ISIS4.

The Liverpool/Lancaster group has gained much experience with irradiated high-speed CCD58 devices over the last years. A CTI model for that 3-phase CCD has been developed using both an analytic approach and FEA device simulation using the ISE-TCAD software. The analytic model is in a good agreement with the ISE-TCAD simulation and provides a good understanding of the underlying processes of charge capture and emission in the context of the device structure. Figure 2.20 shows the FEA simulation for the serial register at three different clock frequencies.

Furthermore, some initial tests using CPC1 have been made in order to determine the correct procedure for CTI measurement. The comparison of the simulations with the experimental data on

radiation damage is crucial for tuning the algorithms and the development of radiation-hard devices. The group will continue this important work with CPC, ISIS and FAPS devices and will be the main centre for LCFI radiation damage studies.

2.6 Work Package 6: Vertex Detector Mechanical Studies

The physics capabilities of an ILC experiment are directly dependent on the amount of material in the vertex detector. In order to reduce tracking errors created by the multiple scattering of particles, the mass inside the vertex tracking region (the beam pipe, the sensors themselves and their mechanical support) must be the minimum necessary to provide robust and stable measurements. Even material external to the active region (bulkheads, external mechanical, service or electrical components) must be minimised due to its effect on the performance of other detector subsystems.

The most challenging part of this overall mechanical problem is the design of the active layers themselves, which must have considerably less material than in previous generations of vertex detectors. The vertex detector at SLD had 0.4% of a radiation length (X_0) per layer, and it is reasonable to aim for an improvement by a factor of four to 0.1% X_0 . This is equivalent to only 100 μm of silicon. Although less material will result in even less multiple scattering, it is unlikely that any lower-mass design could be rigid and stable enough. To achieve even 0.1% X_0 , the sensors would have to be thinned to 20-50 μm at which point they become extremely flexible and fragile. Any support structure will have to be correspondingly light: one or two layers of woven carbon fibre fabric or 200 μm of beryllium for example. The final material budget will be determined by optimising the mechanical characteristics in conjunction with the physics studies in Work Package 1.

The focus of this work package is therefore on developing the technology for approximately 0.1% X_0 detector layers, including the thinning of the silicon, the technology required to support it and the production techniques required to bring them together in a working detector. Any design must result in a stable, rigid detector structure that will survive exposure to the environment at the ILC for the lifetime of the experiment, including frequent cooling to and operation at cryogenic temperatures (if the sensor technology determined in Work Package 2 requires it).

The work package is subdivided into the following tasks:

- 6.1) Detector Layer Support Technologies
- 6.2) Detector Layer Production Methods
- 6.3) Vertex Detector Global Design
- 6.4) Cooling and Thermal Studies

2.6.1 Detector Layer Support Technologies

The various methods and materials for rigidly supporting the sensors within the active volume will be investigated, and the most promising used to build the electrical prototypes for test-beam work. In order to allow sufficient time to develop the production methods (Task 2) the decision between technologies will be taken at the end of the second year of the funding period (Spring 2007).

The most common way of building silicon detector layers is to provide each electrically independent section (one or more silicon sensors connected to a single front-end readout circuit) with its own mechanical support to create a rigid structure (“ladder”). These ladders are then attached to bulkheads to form the active layers (see Figure 2.21). An alternative is to affix all of the electrical sections directly onto a single common support structure (“shell”) that extends through the active region as shown in Figure 2.22.

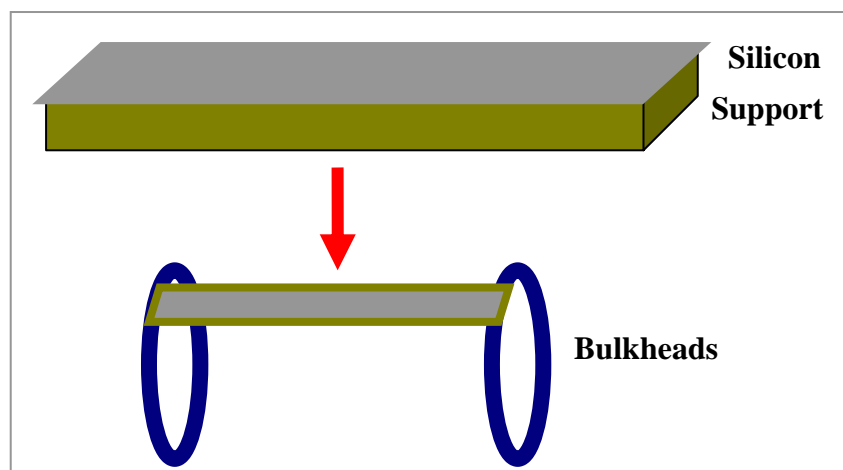


Figure 2.21: Ladder concept, showing separately supported sensors attached to bulkheads.

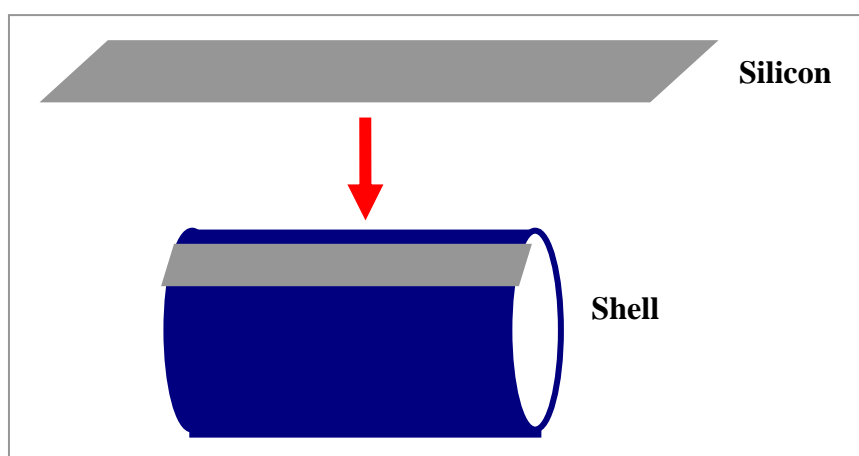


Figure 2.22: Shell concept, showing unsupported sensors attached directly to an integral structure.

The ILC vertex detector is a direct descendent of the highly successful VXD2²⁴ and VXD3¹ at SLD. Both consisted of concentric barrels of detector ladders mounted on beryllium bulkheads. The ladders in VXD3 consisted of a 400 μm beryllium substrate to which 150 μm thick CCDs were attached with pillars of silicone adhesive.

The goal for LCFI is to produce a design with considerably less material than in VXD3 using either much less massive ladders, or sensors attached directly to a low mass shell structure. In addition to having material equivalent to approximately 0.1% X_0 , the detector layers must have uniform thickness to allow reliable estimates of errors in the tracking fits, and be stable over both short and long time scales to allow alignment to be performed and not degrade the intrinsic resolution. They must also be robust enough to survive for the lifetime of the detector despite radiation, thermal cycling and possible mechanical and chemical agents. A final (and far from trivial) requirement is that it has to be possible to assemble these mechanical structures with working sensors to produce real detector layers.

In order to achieve the required stability, the selected support technology will have to provide sufficient stiffness to overcome both external factors (e.g. vibrations induced by cooling processes) and the inherent stresses produced in the sensors by processing. These stresses are currently poorly understood and must be investigated further. In addition, any structure must behave predictably and repeatably under the temperature variations it will experience.

24 G D Agnew et al, Proceedings of the 26th International Conference on High Energy Physics, Dallas 1992 (World Scientific, New York 1992), Vol 2, 1862.

Building the detector layers by stretching 50 μm thick silicon between rigid bulkheads with sufficient tension to keep them rigid was initially considered. Tests showed good repeatability and high stiffness along the length of the silicon, but little control across the sensor width. The intrinsic stresses after processing would therefore produce large deformations and this approach will no longer be considered.

Considerable work has been done on a VXD3-style beryllium/glue/silicon structure. In order to gain the required factor of four in material reduction, the silicon would have to be reduced to 20-30 μm and the beryllium to approximately 100 μm . This would provide sufficient lateral stability to counter the intrinsic stresses in the sensors, but tensioning would be required to provide longitudinal stiffness. Studies have been performed with finite element analysis (FEA) simulations and physical models measured under cooling with a laser scanning system. Both show large buckling effects due to the difference in coefficient of thermal expansion (CTE) between silicon and beryllium (Figure 2.23).

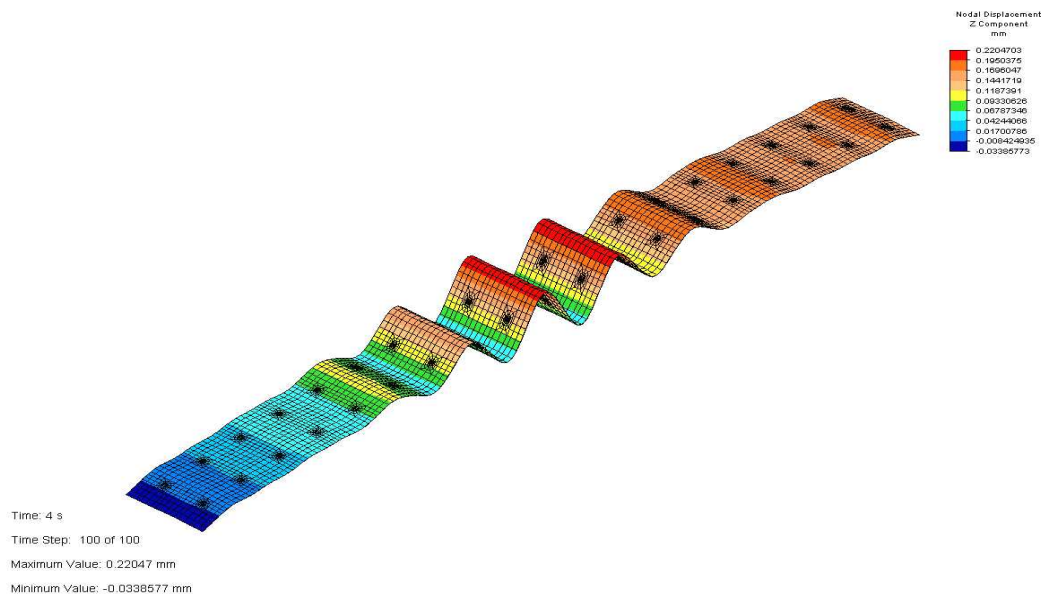


Figure 2.23: FEA simulation of 30 μm thin silicon attached to a beryllium substrate and cooled by 80°C. The peak-to-peak height of the buckles is approximately 200 μm .

Similar structures with different substrate materials to replace beryllium are under consideration. Possibilities include carbon fibre and other composites as well as thin ceramics such as diamond or silicon carbide. Existing expertise within the collaboration as well as collaboration with university engineering departments will help determine if a candidate with a good CTE match and sufficient lateral stiffness can be found. It may also be possible to improve the stiffness by shaping the substrate (e.g. corrugation). The first results from a carbon fibre ladder are compared to those from a steel ladder in Figure 2.24.

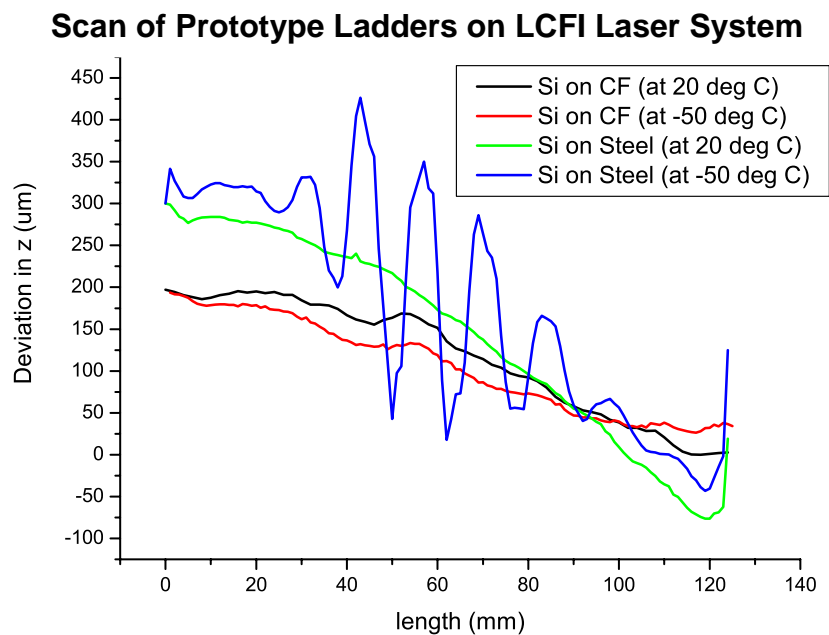


Figure 2.24: Effect of cooling 30 micron thick silicon attached to carbon fibre, compared to silicon attached to steel.

Eliminating the need for longitudinal tensioning will enable the reduction of material in the regions at the ends of the ladders. Sufficient stiffness may be provided by a silicon carbide foam substrate, or by a sandwich-type structure in which two “skins” of silicon (one of which would be the sensor) are separated by a low density core material. Candidates for the core could include reticulated vitreous carbon foam, rigidised felts or even micromechanical structures.

Sensors could be attached directly to a carbon fibre shell, but there is worry that there could be severe distortions if one or more sensors have to be powered off. These effects will be studied by FEA to determine if this will be feasible.

The following subtasks are defined:

*Task 6.1.1: **Novel material properties:*** Expertise must be gained in the handling, mechanical properties and thermal behaviour of new materials such as foams and composites, in order to determine their suitability for use in sensor supports.

*Task 6.1.2: **Ladder prototyping:*** Ladder-style sensor support concepts must be fully tested by a combination of building models and FEA studies. Thermal and mechanical properties will be tested as well as robustness, radiation hardness and aging to eliminate any flawed designs and determine which is most promising

*Task 6.1.3: **Shell studies:*** Modelling of possible shell-type support schemes will be carried out with supporting FEA simulations to determine if there are any advantages or disadvantages over ladder-style schemes and investigate possible designs.

*Task 6.1.4: **Silicon Stress:*** Intrinsic stress in processed silicon will be investigated and quantified. This is required for accurate model building and FEA analysis in 1.2 above, and will be a major factor in determining the required stiffness of the structures.

2.6.2 Detector Layer Production Methods

Fully-functioning detector prototypes must be constructed for beam tests, which means devising various techniques for assembly and processing. The details will depend on the technology chosen in Task 1, and sufficient understanding of the processes required must be maintained to ensure that the technology chosen is compatible with the ultimate goal. After the technology choice, detailed

procedures and fixture designs will be devised and tested and ultimately the test structures will be prototyped.

Understanding of general issues such as robustness and handling procedures will be gained from samples and models. Additional detailed studies will be required to investigate:

Task 6.2.1: Adhesives. An adhesive suitable for use with the chosen support technology and compatible with all aspects of production and operation will be found. Silicone elastomers, favoured for use with a beryllium substrate, are unlikely to prove ideal for a carbon foam sandwich. Factors that have to be considered are

- Elastic modulus
- Curing method
- Adhesion strength
- Failure mechanisms
- Viscosity
- Aging
- Radiation hardness
- Activation

These will be investigated in the lab, using glue samples and prototype ladders. In addition, the thickness and pattern of glue used will be studied in simulation and prototypes.

Task 6.2.2: Silicon thinning. A reliable and affordable method of thinning the sensors to the required thickness will be found. Mechanical thinning of silicon wafers to $\sim 100\ \mu\text{m}$ is widely available, but the technology to thin further, possibly down to a $20\ \mu\text{m}$ epitaxial layer is currently limited to a few specialist companies.

Task 6.2.3: Bump bonding compatibility. A scheme for production of complete electrical ladders, including flip chip bonding, will have to be worked out with the contractors. It will have to be tested and shown to be viable.

Task 6.2.4: Wire bonding. Connections between the sensor and external services and readout will have to be made by wire bonding. Some of the candidate substrate technologies could present difficulties with this process, so specific procedures will be developed and tested.

2.6.3 Vertex Detector Global Design

Within the scope of the R+D phase of LCFI, global design efforts are of use to establish the feasibility of the various support technologies. Designs for the overall detector layout, detector positioning, end regions and ladder attachment will be worked out in sufficient detail to ensure that any support technology is ultimately feasible before the technology choice in Task 1. Some additional work will be performed to minimise the material outside the active volume and investigate options for services.

Work in this area is divided into three subtasks:

Task 6.3.1: End regions. The design and layout of the ladders or shells outside the active region will be investigated. The placement of components, extra structural material and attachment to the main detector structure must be developed depending on the choice of support technology.

Task 6.3.2: Structure. Preliminary designs for the major mechanical components of the vertex detector (the beampipe, bulkheads, outer screen and cryostat, if necessary) will be prepared. The thickness and structure of the beampipe has a direct impact not only on physics, but also on the external mechanics of the bulkheads and the outer shell, which may also act as a Faraday Cage. The design of the bulkheads will also have to be compatible with the ladder or shell design, and mock-ups of the bulkheads will be used to test ladder mounting schemes. The characteristics required of the cryostat will depend on the power dissipation and operating temperature of the sensor technology chosen in Work Package 2.

Task 6.3.3: Services. Preliminary concepts for the provision of gaseous and liquid cooling will be worked out. The details, including whether liquid cooling is required, will depend upon the

choice of sensor and the location and power consumption of any external electronics (Work Packages 2, 3, 4).

2.6.4 Cooling and Thermal Studies

Specific preliminary thermal studies will be performed to support work in other areas. These will include FEA studies on the effect of very low duty cycles, and physical and 3D computer modelling of cooling via cold gas flow. The details of power dissipation and duty cycle, and the location of any support electronics is dependent on Work Packages 2, 3 and 4. More specific modelling (computational and physical) will be performed once these are known to determine the parameters for Task 3.3.

2.7 Work Package 7: Test-beam and EMI Studies

At the end of the five years covered by this proposal, our goal is to test full size prototype vertex detector ladders in test-beams. The data obtained from these test-beams will be crucial for assessing the relative performance and capabilities of the different sensor technologies. Furthermore, experience gained from the construction and mounting of the prototype ladders will allow us to refine the design of the final vertex detector in order to maximise its mechanical robustness whilst maintaining the required physics performance. This test-beam work is crucial for ensuring that the optimum sensor technology is chosen. These tests are therefore vital to the ultimate success of the vertex detector.

The international vertex detector community will make the choice of technologies for the ILC vertex detectors in 2009/2010. The only way to assess the relative strengths of the competing sensor designs will be to take data with fully assembled prototype ladders in test-beams²⁵. This will require the development of a portable test-stand with readout electronics and support infrastructure (including cryogenics, data acquisition and any necessary triggering and alignment systems) that can be assembled and commissioned in the UK before being shipped out to the test-beam site. The test-beam studies will establish the performance characteristics of the sensors – including point resolution, performance of the readout chip data-sparsification algorithms, effects of high magnetic fields and noise susceptibility.

The beam-tests of ladders will naturally occur towards the end of the proposal period when complete sensors and their support infrastructure become available (see WP2 and WP5 for details). However before these tests, we plan detailed investigations into the environment of the interaction region to identify factors which may impact on the choice of sensor technology.

Beam related backgrounds have long caused problems for experiments in particle physics. Wake-fields – generated by the passage of an intense bunch of relativistic, charged particles through non-uniform accelerator structures – especially their higher order modes, can generate considerable broadband radio frequency radiation inside the beam pipe. This RF can cause operational problems for both the accelerator and the detectors.

In accelerators, problems such as poor vacuum due to heating of the beam pipe^{26,27} or machine elements have been observed. Detectors have suffered from electromagnetic energy, generated by the beam, escaping from the beam pipe and interfering with their front-end readout electronics¹ and amplifiers (EMI). Due to the importance of these beam-induced electromagnetic fields for the very short intense bunch structure of the ILC there is already much ongoing study into RF generation inside the beam pipe of the proposed accelerator design. The understanding of EMI escaping from the beam pipe is far less advanced. This is partly because energy escaping from the beam pipe is not directly relevant to machine operation, but also because such leakage is difficult to model.

²⁵ http://www-lc.fnal.gov/lc_testbeams/tbpage.html

²⁶ Higher order mode heating of the HERA II beampipe, <http://www.cerncourier.com/main/article/45/2/17>

²⁷ S. Ecklund et al., *High Order Mode Heating Observations in the PEP-II Interaction Region*, [SLAC-PUB-9372](#) (2002).

Experience at SLD has shown that beam induced EMI problems can render pixel-based silicon vertex detector readout electronics inoperative when particle bunches are interacting within the detector. Furthermore, different detector technologies²⁸ are expected to have different sensitivities to EMI. Hence, to choose the appropriate technology and to guide the design of the interaction region beam-pipe, it is vital to understand beam induced EMI in much more detail than presently possible. Predicting the effects of EMI on a detector due to beam induced RF requires knowledge of the spectrum generated inside the beam pipe, the attenuation of the RF by the beam pipe, or any joins or ports in the beam pipe, the coupling of the radiation to the detector and finally the sensitivity of the detector.

The following sections outline the tasks that we intend to undertake over the period covered by this proposal.

2.7.1 EMI Test-Beams

From the end of 2005 we have a program of work to develop and test the sensors necessary to measure beam-related EMI. The first stage, in collaboration with colleagues from the international vertex detector community, is the instrumentation of the beam-line around the Final Focus Test Beam (FFTB) facility at SLAC with antennae in order to determine the electric and magnetic fields outside the beam pipe and analyse their frequency and power spectra. The measurements made here would be carried out in parallel with normal operation of the FFTB, with any modifications to sensors or installation of equipment being done during regular accesses to the FFTB area. The instrumentation and expertise developed at the FFTB will subsequently be used to measure EMI at a dedicated test-beam using the End Station-A beam-line. The FFTB is expected to resume operation towards the end of 2005.

The End Station-A test-beam at SLAC (ESA) is an ideal location for dedicated EMI studies. The bunch intensity ($0.75\text{--}2.0\times 10^{10}$ electrons) is close to that planned for the ILC and the bunch length can be adjusted in the range $100\mu\text{m} - 1000\mu\text{m}$ relevant to the ILC. It is expected²⁹ that the increase in beam induced RF with beam energy will saturate for particle velocities greater than $\beta\approx 100$, hence tests at relatively low beam energies should give valuable information about ILC operation. The ESA test-beam will certainly be available until the end of operation of the b-factory in 2008 and probably longer.

In SLD beam-induced EMI caused saturation of analogue signals during beam-crossings in VXD2 and failure of a data-link in the readout for a short period during beam-crossing in VXD3. These problems were present even if only one beam was present, ruling out ionizing radiation from the interaction as the cause of the problem. The vertex region of SLD (the R20 module) was stored after the experiment was decommissioned. The R20 module will be used in the EMI studies as a practical example of the complex structure around an experimental interaction region. The R20 module and SLD VXD3 vertex detector will be used to reproduce the problems experienced during the operation of SLD and to determine their cause. The tools developed at the FFTB will be used to instrument the R20 module and investigate the specific problems induced in the VXD3. The aim is to identify if the source of the EMI is local or from upstream accelerator structures. For example the complex shaped beam pipe in the R20 module will be replaced by a simple, smooth tube – this should lead to valuable insights on locally generated EMI. We anticipate this first EMI test-beam would take place early in 2006.

Results from these studies will be compared with simulations and the simulations in turn used to devise structures which will help minimise EMI effects. Another set of beam tests towards the end of 2006 will test these structures and provide more input for improving the simulation.

²⁸ The column-parallel CCD (CPCCD), ISIS and FAPS devices are expected to have different sensitivities to EMI. In particular, FAPS devices which rely on the storage of voltages in the pixel may suffer more from EMI effects than the CPCCD/ISIS sensors which store charge.

²⁹ N. Sinev, private communication

2.7.1.1 Modelling Beam Induced RF and Sensor Susceptibility

Simulations of beam induced RF *inside* the beam pipe will be performed as part of the ILC design process and test-beam measurements³⁰ will be made as part of the design process for the final beam delivery system³¹. However, these studies do not cover RF leakage out of the beam pipe, so it will be necessary for us to develop the tools and expertise to simulate this electromagnetic leakage.

RF/EMI simulation software is commercially available and has become increasingly sophisticated as the needs of industry to model EMI have increased. Packages such as CST Microwave studio (MAFIA³²) and GDFIDL³³ are in use at CERN and CCLRC for EMI modelling. These finite element (FEM) and finite difference time domain (FDTD) packages, in use within the HEP community, provide a framework for EMI and RF simulation and are an appropriate starting point in the search for applicable software. A possible alternative could be to use the FDTD package developed by the RF structures group at the Electrical Engineering department of the University of Bristol. Irrespective of the simulation framework ultimately chosen, the geometry and structures of the ILC interaction region will need to be implemented into the package.

In principle, it is possible to model the RF leakage through flanges, bellows, ports for laser-wires and other similar structures. In practice this leakage will depend on precise details of the geometry and materials used in these features and any model will have to be verified and refined against experimental measurements. Expertise in this area already exists at Bristol in the RF systems group (part of the department of electrical and electronic engineering). We will develop software models of RF leakage based on the EMI test-beam data with expert advice from the RF systems group. These models will be used to develop an understanding of the EMI environment that the vertex detector will encounter at the ILC. In conjunction with the simulation of the beam related EMI it will also be vital to understand the susceptibility of the various sensor technologies to this EMI, since this may have a material effect on technologies with in-sensor charge-to-voltage conversion and storage.

2.7.1.2 Measuring Sensitivity of Sensors and Readout Electronics to EMI/Noise

During integration tests for the LHC detectors' electronics the need has arisen to be able to assess the various modules' sensitivity to noise³⁴. Noise induced by other electronic devices in close proximity to high-speed detectors has been shown to severely degrade the performance of some systems when operating in an integrated environment even though they function in stand-alone tests. Consequently, the LHC experiments have developed methods to inject noise into electronic systems, through the use of cable clamps and signal generators, in order to assess components susceptibility to noise and understand how to mitigate its effects. We propose build on this expertise and apply it directly to the sensors, drive and readout electronics in order to assess their susceptibility to external noise. This work will run concurrently with the efforts to understand the sensitivity of the detectors to beam related EMI as the measured RF spectrum will be needed to guide the laboratory EMI testing.

The noise susceptibility of the sensors and electronics will be characterised using known RF signals injected into cables. Since the EMI test-beams will provide detailed information about the frequency and power spectra of the electromagnetic environment that the sensors will be exposed to, combining these measurements with the noise susceptibility measured from direct signal injection will largely characterise the sensitivity of the sensors to their operating environment in a reproducible and controlled environment. Of course, testing the full prototype ladders in a test-beam is the only way to completely understand the EMI susceptibility of the final design, but by carrying out these measurements beforehand we will ensure that the ladders are as robust as possible against EMI effects before being taken to the test-beam. We anticipate an initial period, during which the tools are

³⁰ <http://www-project.slac.stanford.edu/nlc/testfac/FFTB.html>

³¹ See, for example, <http://www.eurotev.org>

³² <http://www.cst.com/Content/Products/MAFIA/Overview.aspx>

³³ <http://www.gdfidl.de/>

³⁴ See, for example, <http://cms-emc.web.cern.ch/cms-emc/>

assembled, followed by testing and characterisation as working prototype sensors become available. The ability to carry out reproducible, bench-top testing for EMI and noise robustness will be an essential tool for the worldwide vertex detector community, and we expect that our expertise will have much wider applicability than just the studies needed by LCFI.

2.7.2 Prototype Ladders in Test-Beams

As stated in the introduction, the ultimate goal of LCFI at the end of the next five years is to build and assemble prototype ILC vertex detector sensor ladders and evaluate their performance in test-beams. Without these test-beam studies, it will be impossible to evaluate the performance of the different sensor technologies, data sparsification algorithms and readout chip performance in realistic operating conditions. The ultimate choice of technology for the ILC experiments' vertex detectors will be determined by the data gathered during these test-beams, so we must be fully prepared for them in order to maximise the amount of high-quality information recorded.

Experience at other test-beams has shown that it is vital to have at least two test-beam slots reasonably close together – preferably within a year of each other. This allows for an initial period of commissioning of the detectors and readout systems, followed by analysis of the data, during which simulations and tools are updated and improved. For example, the effect of high (~ 5 T) magnetic fields on hit resolutions can only be quantified at a test-beam, as can the overall point resolution of the sensors. Subsequent test-beams will then be used to gather large, high-quality data sets from which a very detailed understanding of the complete detector and electronics chain can be achieved. It is these results that will pave the way to the technology choice for the final vertex detector design. We anticipate using the existing test-beam infrastructure at SLAC (including silicon telescope for beam alignment) and possibly the DESY test-beam if the EUDET framework six proposal is funded.

The test-beam studies will be the culmination of the preceding years of development work within LCFI. Preparation for the test-beams must begin far enough in advance of the first slot in order to ensure that the necessary infrastructure is in place – for example, external silicon telescopes, computing infrastructure and interface electronics must be ready for day one of test-beam operation. Some items will naturally be provided by other members of the vertex detector community, whilst others will have to be developed. It will take a minimum of six months prior to the first test-beam to build any components that we require to interface with the test-beam infrastructure. The necessary DAQ and readout electronics for the test-beams will be developed within WP4, whilst deployment and interface work will be undertaken as part of this workpackage. We anticipate that this preparatory work would begin around the middle of 2007, leading to the first test-beam towards the end of 2007 for CPC3. This first test-beam slot would then be followed by further data-taking commencing in the second half of 2008 and continuing for tests of CPC4 and ISIS at the end of the proposal period.

2.8 Work Package 8: Financial and Management

The detailed management structure of LCFI is discussed in the Management Plan in Section 3.